High-Yield Repairing Algorithms for 2D Memory with Clustered Faults

Tsung-Chu Huang (黃宗柱)
Department of Electronic Engineering
National Changhua University of Education

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Outline

- Introduction
  - Introduction to Memory
  - Introduction to Magnetoresistive RAM
  - Introduction to Memory Test
- Fault-Distributive Modeling
- Previous Work
- Effect-Cause Fault Analysis
- Proposed HYPERA
  - Remapping Architecture
  - Repairing Algorithms
  - Redundancy Analysis
- Conclusions

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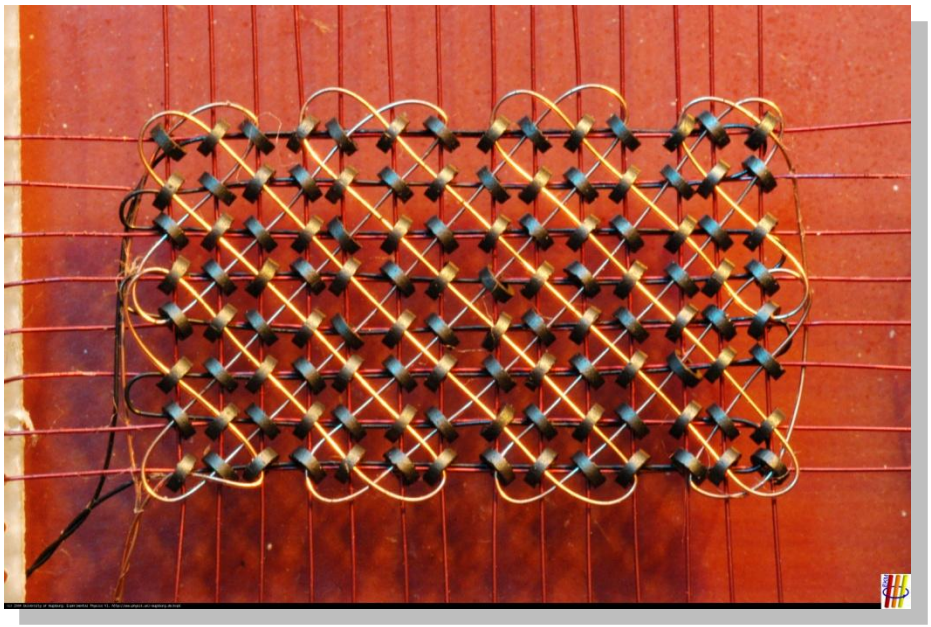
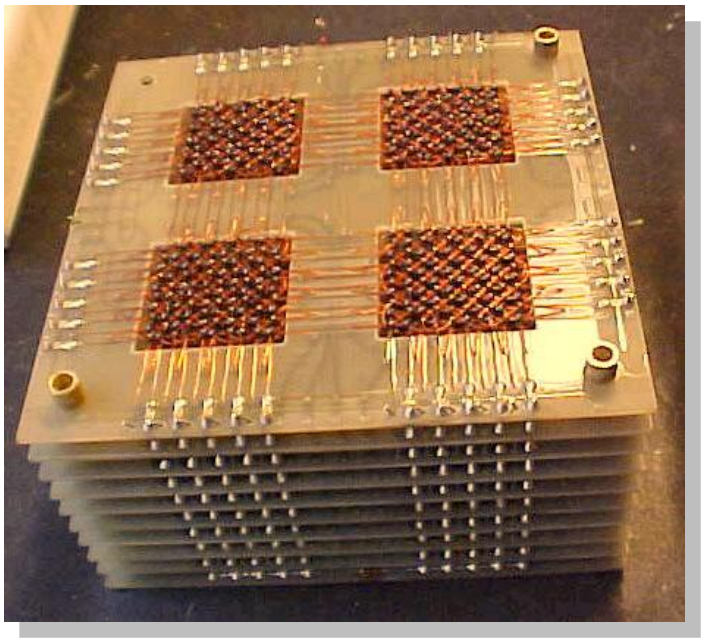
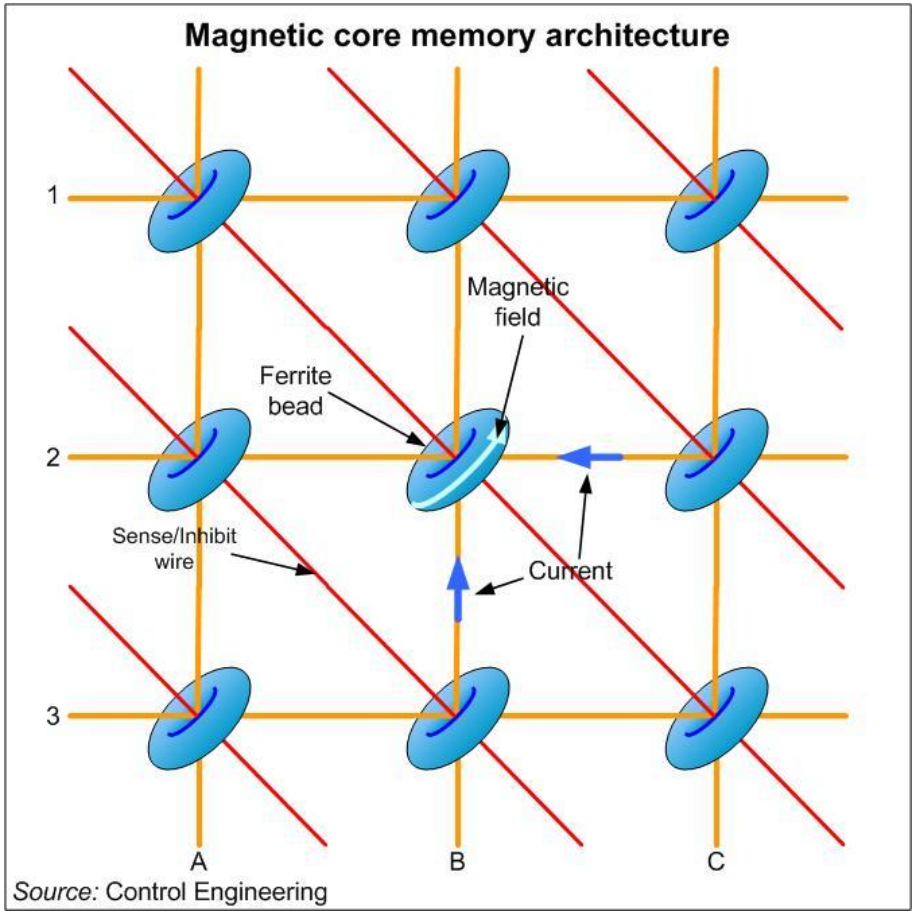
Magnetic Core RAM





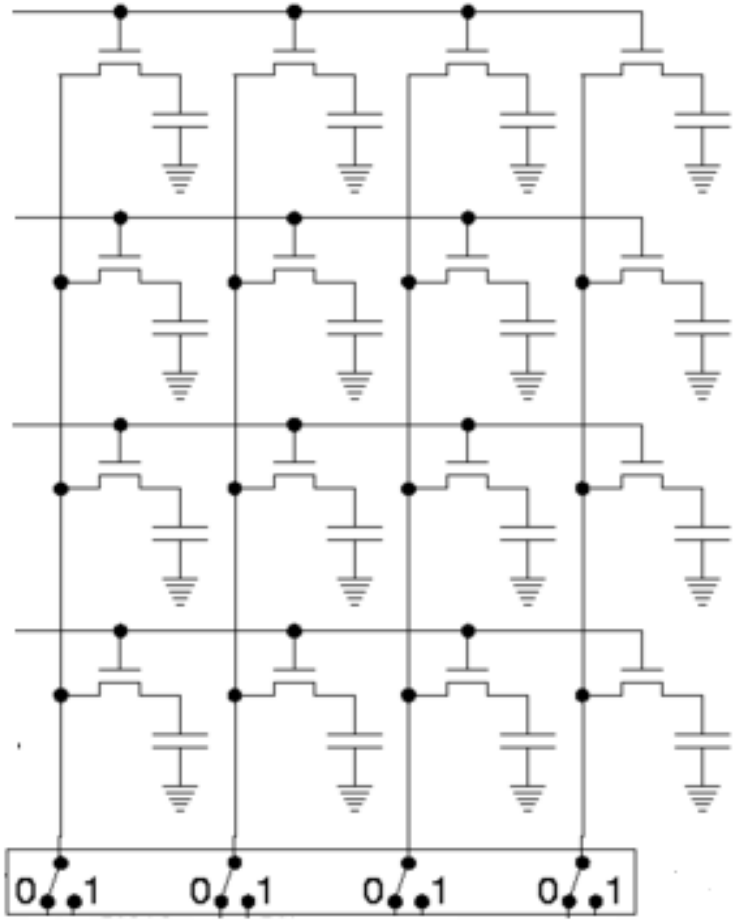
By the early 1960's, Magnetic Core RAM became largely universal as main memory, replacing drum memory.

Magnetic Core RAM



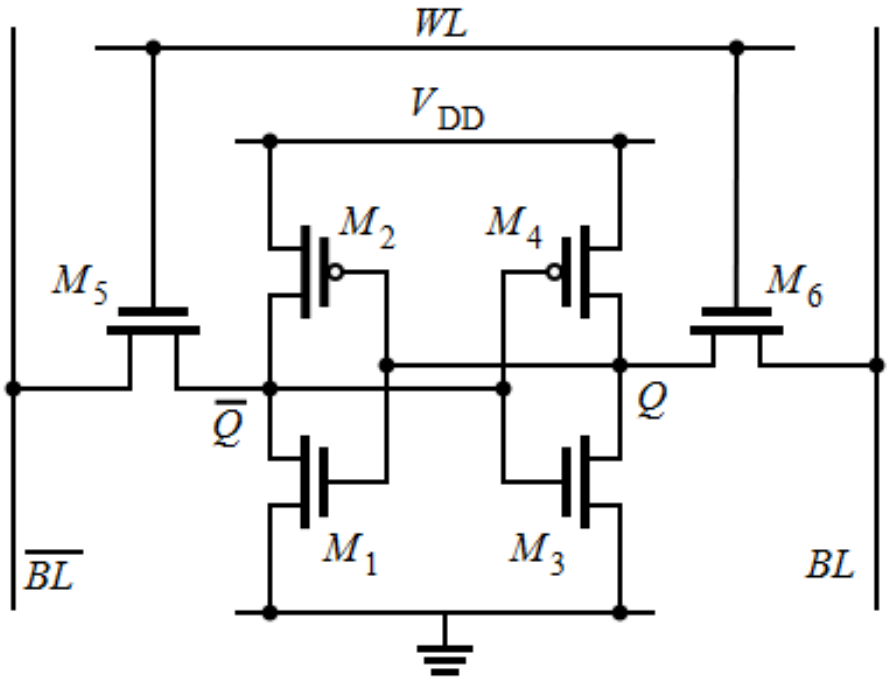
- The memory cells consist of wired threaded tiny ferrite rings (cores).
- X and Y lines to apply the magnetic filed.
- Sense/Inhibit line to 'read' the current pulse when the polarization of the magnetic field changes.

Dynamic RAM (DRAM)



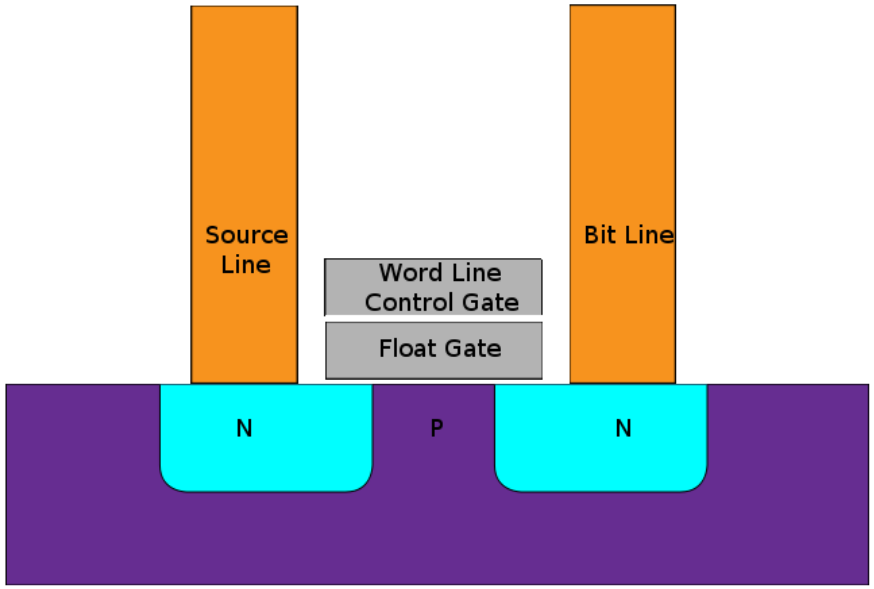
- Each bit of data is stored in a separate capacitor within an integrated circuit
- Volatile
- The highest density RAM currently available
- The least expensive one
- Moderately fast

Static RAM (SRAM)



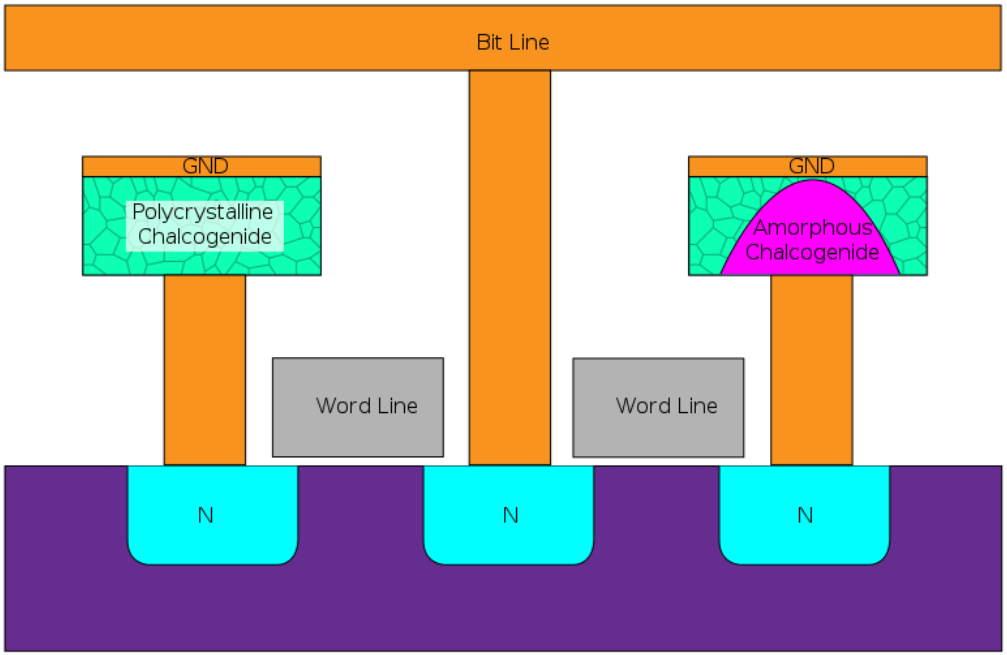
- Each bit is stored on four transistors that form two cross-coupled inverters
- Expensive
- Volatile
- Fast
- Low power consumption
- Less dense than DRAM

Flash Memory



- Stores information in an array of memory cells made from floating-gate transistors
- Cheap
- Non-volatile
- Slow
- Enormously durable
- Limited endurance

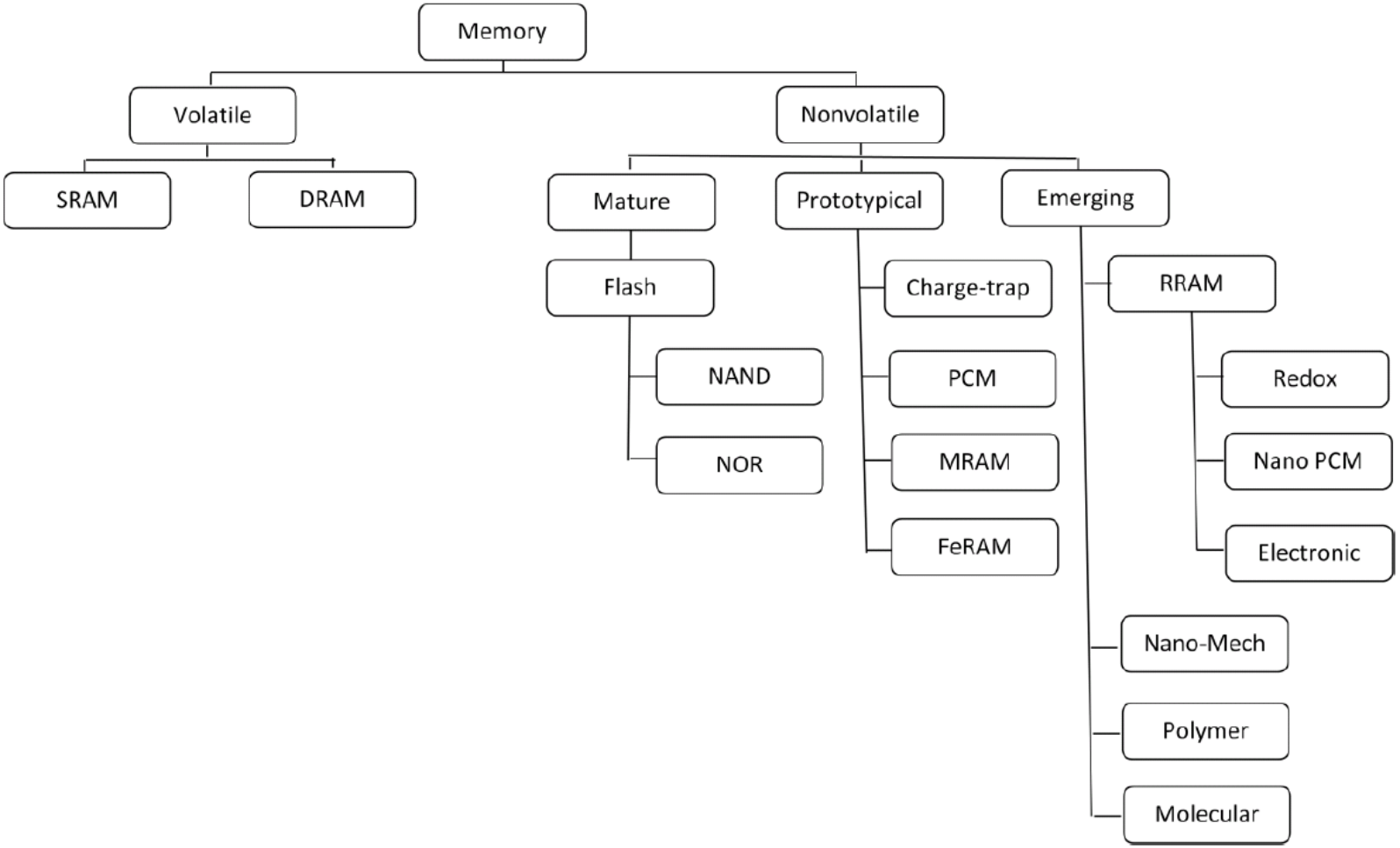
Phase Change Memory (PCM)



- Changes amorphous or crystaline phases by thermal current
- Emerging
- High density
- Nonversatile

(source: wikipedia)

Memory Families



(Source: ITRS2010)

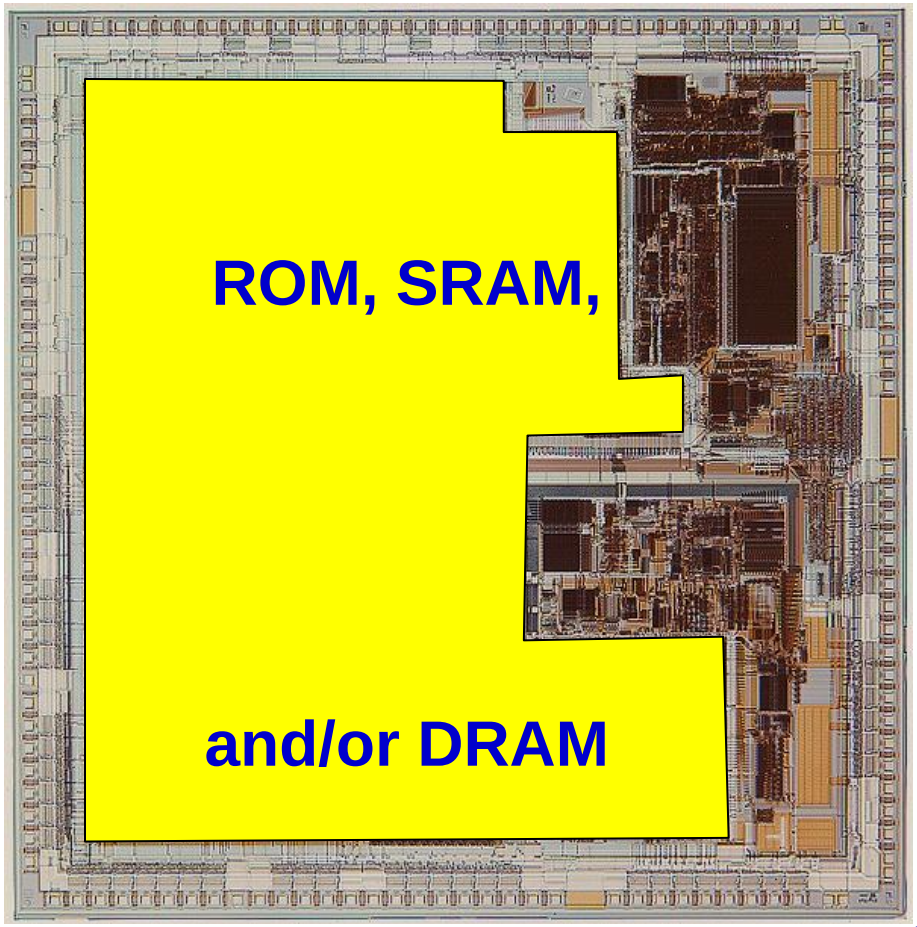
Memory Families

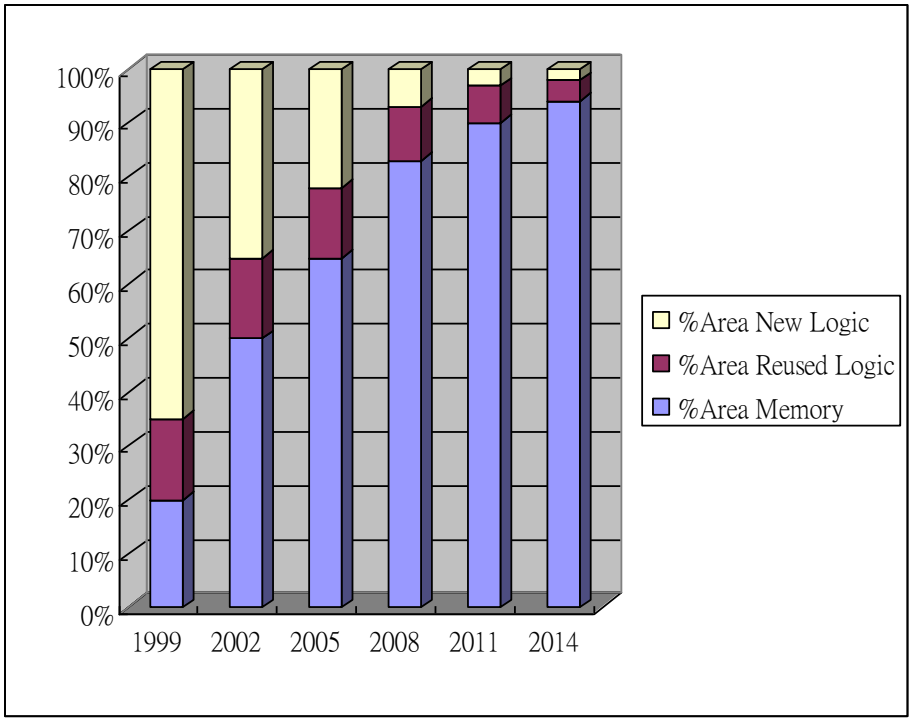
		Baseline Devices					Prototypical Devices [A]			
		DRAM		SRAM [C]	Floating Gate [E]		Trapping Charge [G]	FeRAM	MRAM	PCM
		Stand-alone [A]	Embedded [C]		NOR	NAND				
Storage Mechanism		Charge on a capacitor		Inter-locked state of logic gates	Charge on floating gate		Charge trapped in gate insulator	Remnant polarization on a ferroelectric capacitor	Magnetization of ferromagnetic layer	Reversibly changing amorphous and crystalline phases
Cell Elements		1T1C		6T	1T		1T	1T1C	1(2)T1R	1T1R
Feature size F, nm	**2007**	68	90	65	90	90	65	180	90	65
	2022	12	25	13	18	18	10	65	22	18
Cell Area	**2007**	$6F^2$	$12F^2$	140 F^2	10 F^2	5 F^2	$6F^2$	$22F^2$	$20F^2$	$4.8F^2$
	2022	$6F^2$	$12F^2$	140 F^2	10 F^2	5 F^2	$5.5F^2$	$12F^2$	$16F^2$	$4.7F^2$
Read Time	**2007**	<10 ns	1 ns	0.3 ns	10 ns	50 ns	14 ns	45 ns [I]	20 ns [M]	60 ns [P]
	2022	<10 ns	0.2 ns	70 ps	2 ns	10 ns	2.5 ns	<20 ns [J]	<0.5 ns	< 60 ns
W/E Time	**2007**	<10 ns	0.7 ns	0.3 ns	1 □s/ 10 ms	1/0.1ms	20⁄s/20ms[H]	10 ns [K]	20 ns [M]	50/120ns[P]
	2022	<10 ns	0.2 ns	70 ps	1 □s/ 10 ms	1 ms/ 0.1 ms	~10⁄s/10 ms	1 ns[J]	<0.5 ns [N]	<50 ns
Retention Time	**2007**	64 ms	64 ms	[D]	>10 y	> 10 y	>10 y	>10 y	>10 y	>10 y
	2022	64 ms	64 ms	[D]	>10 y	> 10 y	>10 y	>10 y	>10 y	>10 y
Write Cycles	**2007**	>3E16	>3E16	>3E16	>1E5	>1E5	1.00E+05	1.00E+14	>3E16	1.00E+08
	2022	>3E16	>3E16	>3E16	>1E5	>1E5	1.00E+06	>1E16	>1E16	1.00E+15
Write Operating Voltage (V)	**2007**	2.5	2.5	1.1	12	15	7–9	0.9-3.3	1.5 [M]	3 [P]
	2022	1.5	1.5	0.7	12	15	6-Apr	0.7–1	<1.5	<3
Read Operating Voltage (V)	**2007**	2	2	1.1	2	2	1.6	0.9–3.3	1.5 [M]	3
	2022	1.5	1.5	0.7	1.1	1.1	1.1	0.7–1	<1.8	<3
Write Energy (J/bit)	**2007**	5E-15 [B]	5.00E-15	7.00E-16	>1E-14 [F]	>1E-14 [F]	1E-13 [H]	3E-14 [L]	7E-11 [A]	5E-12 [Q]
	2022	2E-15 [B]	2.00E-15	2.00E-17	>1E-15 [F]	>1E-15 [F]	>1E-15	5E-15 [L]	2E-11 [A]	<1E-13 [Q]
Comments					Multiple-bit potential	Multiple-bit potential	Multiple-bit potential	Destructive read-out	Spin-polarized Write has a potential to lower Write current density and energy [O]	Multiple-bit potential

(Source: ITRS2010)

Importance of Memory Repairing

- ITRS: Memory occupies 87% by 2014
- TISA: > 33% of Semiconductor product





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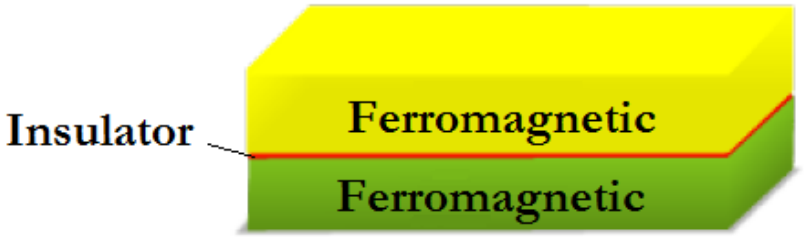
Tunnel Magnetoresistance (TMR)

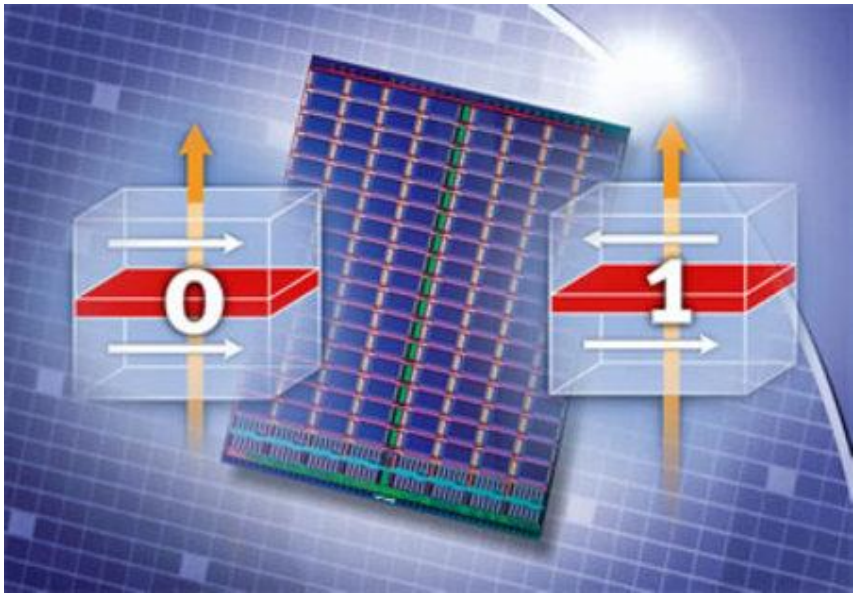
Two thin films of altering ferromagnetic materials and an insulating spacer.

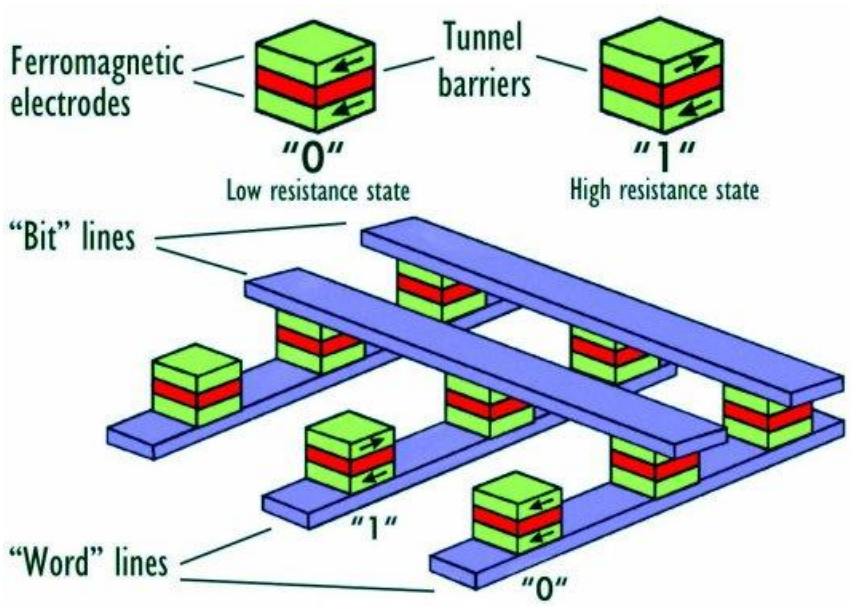


*Fe/MgO/Fe junctions reach over **200%** decrease in electrical resistance at room temperature*

***600 (room temperature)-1100 (4.2 K) %** TMR at junctions of CoFeB/MgO/CoFeB*

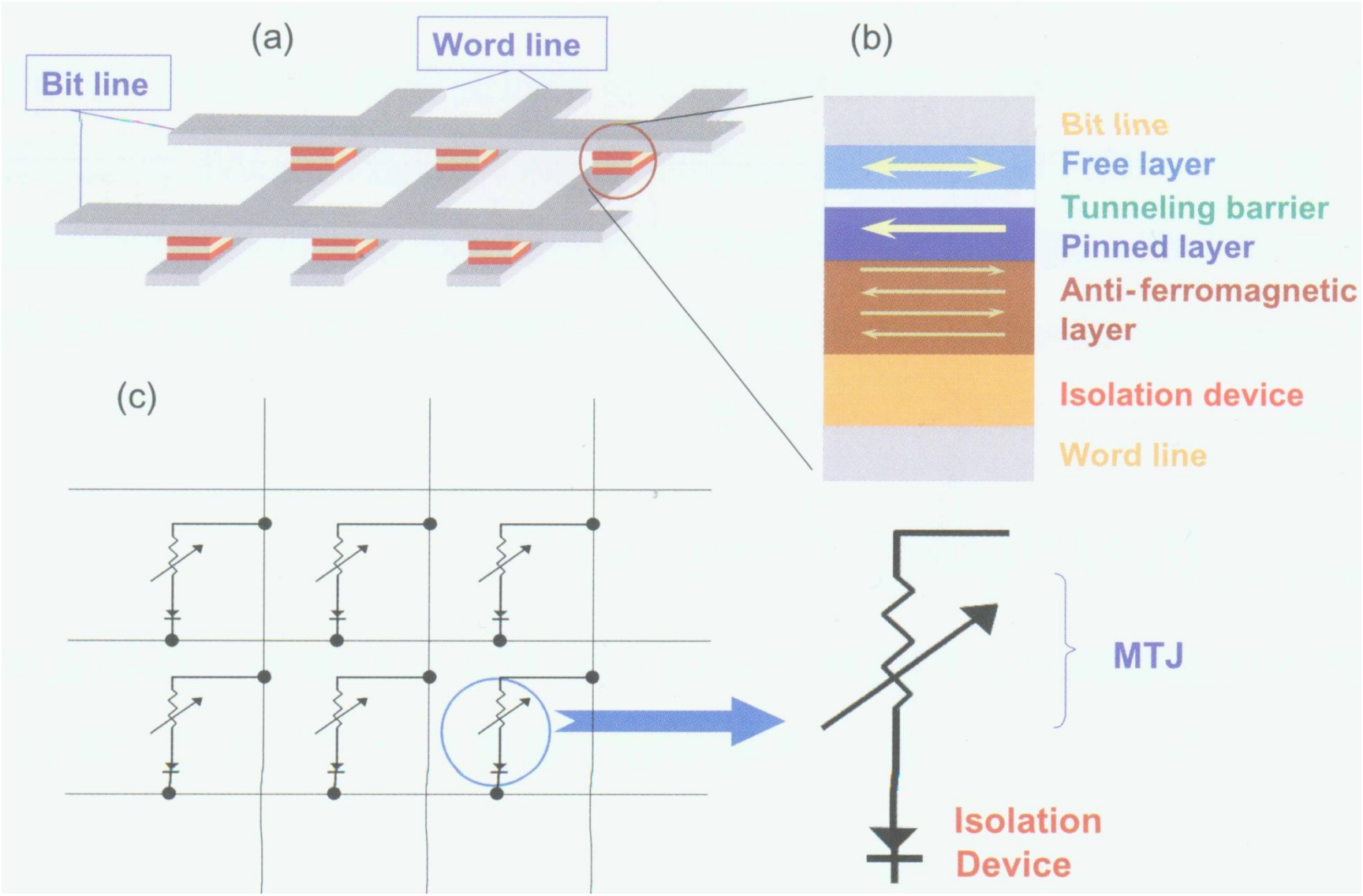
MRAM



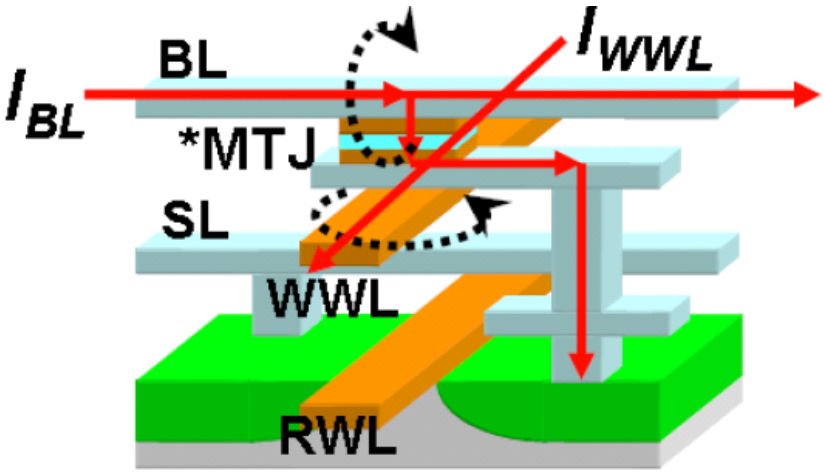


One of the two plates is a permanent magnet set to a particular polarity, the other's field will change to match that of an external field.

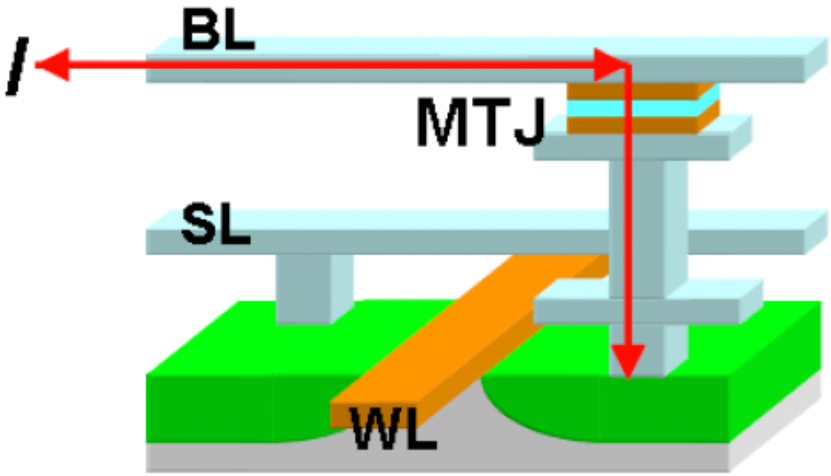
Basic NOR-Type Array



Basic MRAM Structures

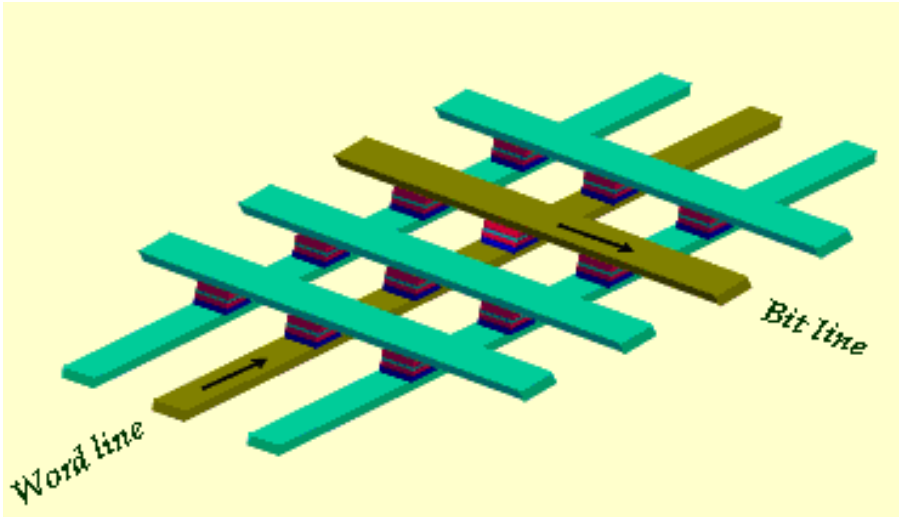


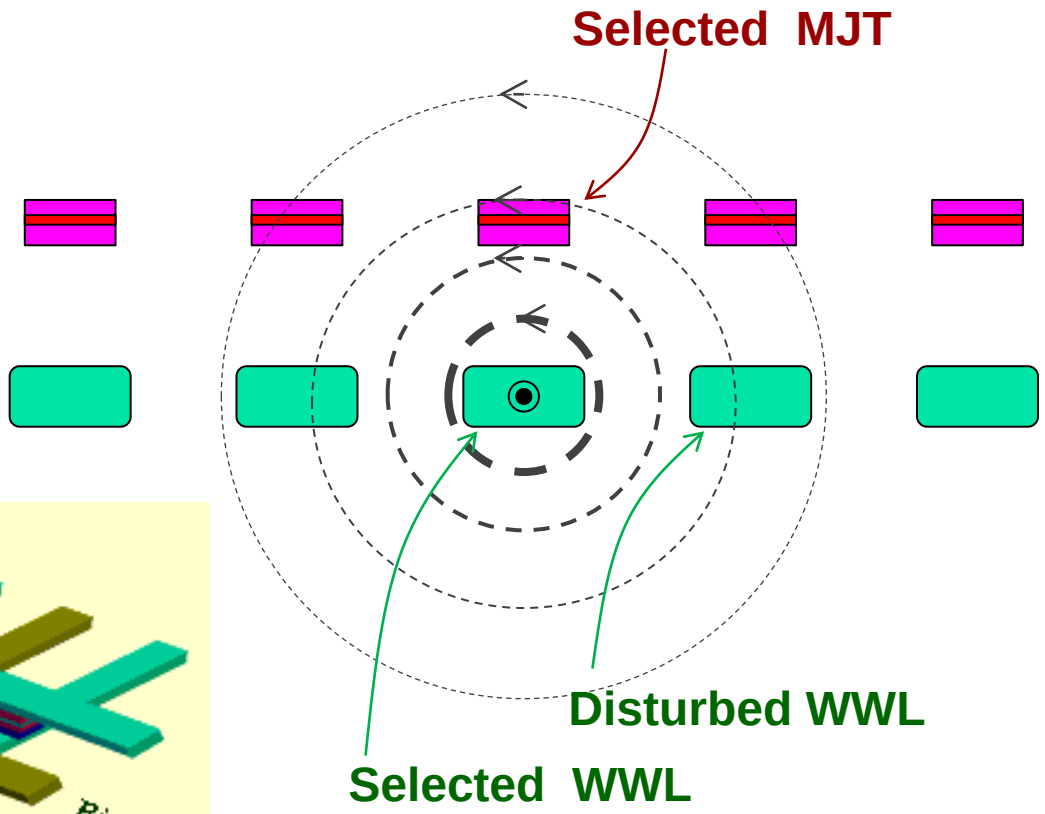
Conventional Structure with WWL + RWL



Single WL Structure

Fault Model





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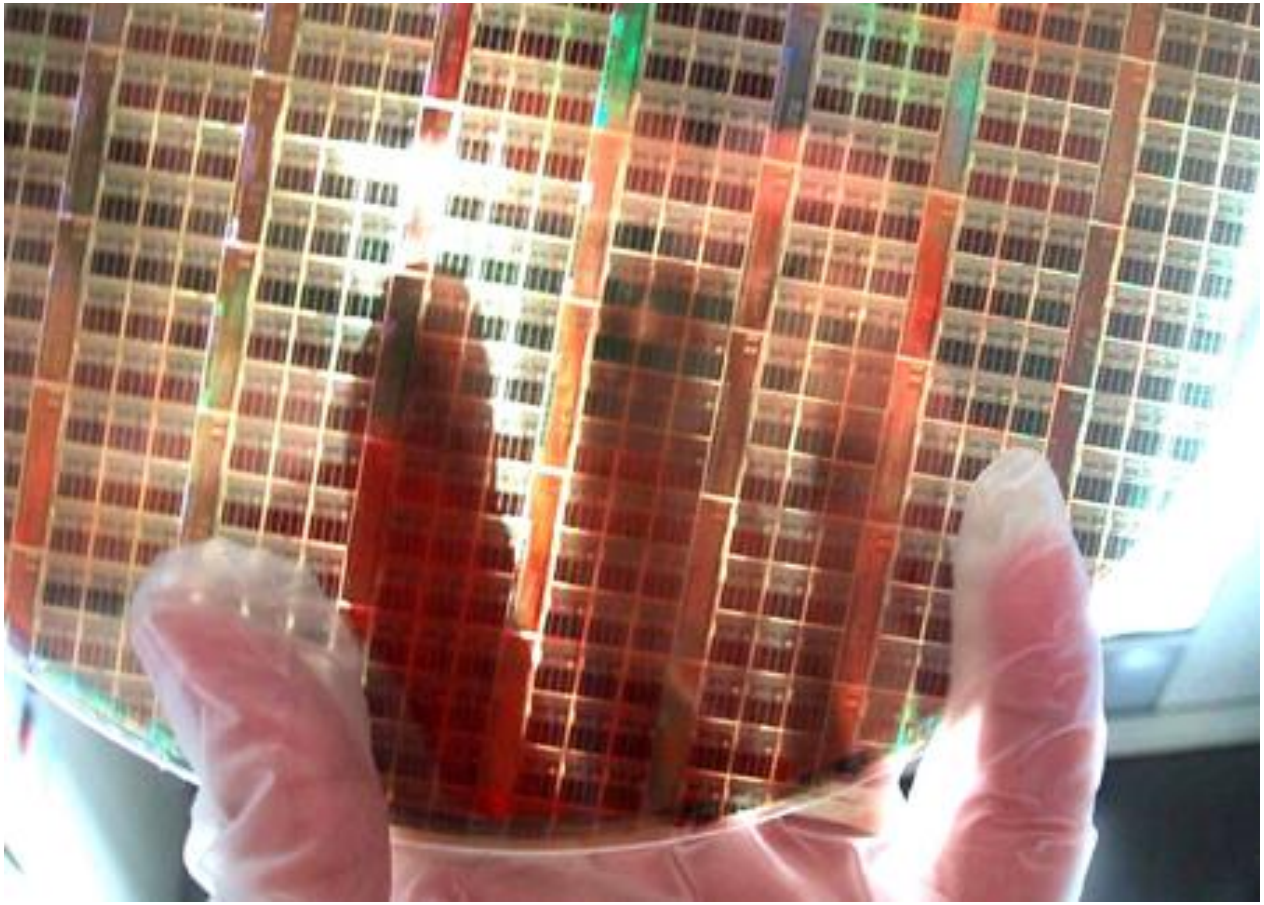
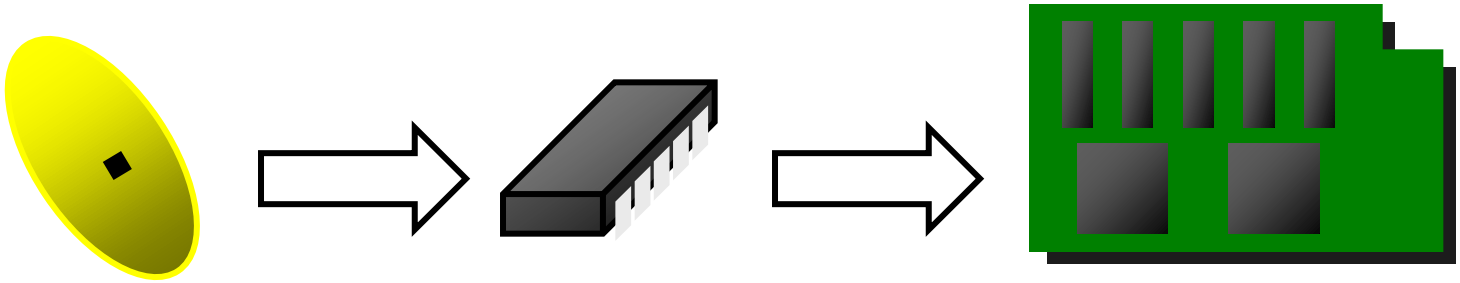
Yield 良率

- ➔ $USD



Importance of Memory Test

- Without test at stage k
  - Cost wasted: $(1-Y)(P_{k+1}-P_k)$

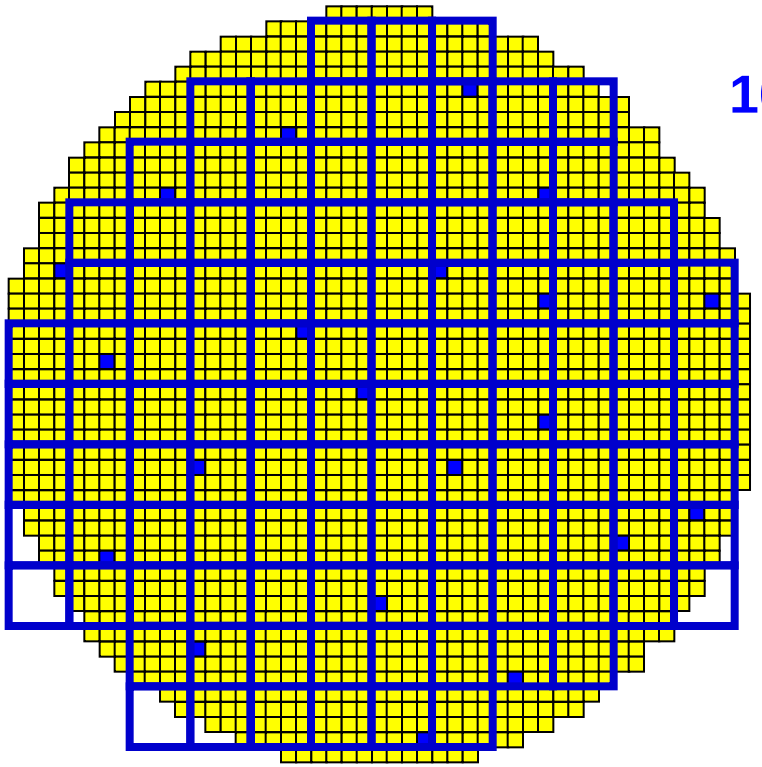


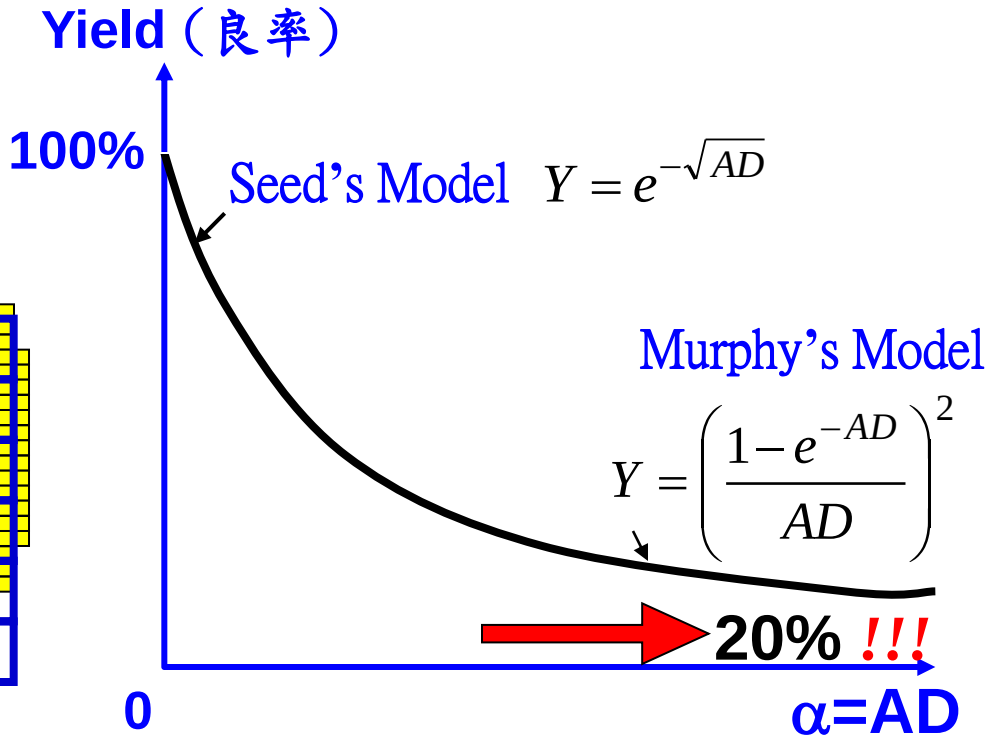
$1 $10 $100

Rule of Tens

Importance of Memory Repair

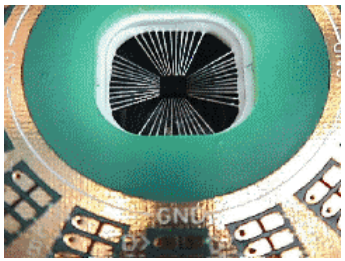
- **When chips are very small, assume the probability of defected chip is α**
  → Y=1- α

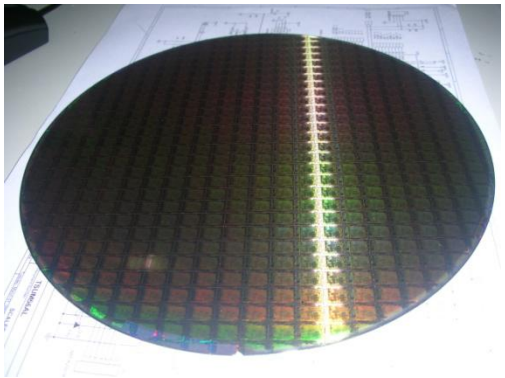




Wafer Test

Tester



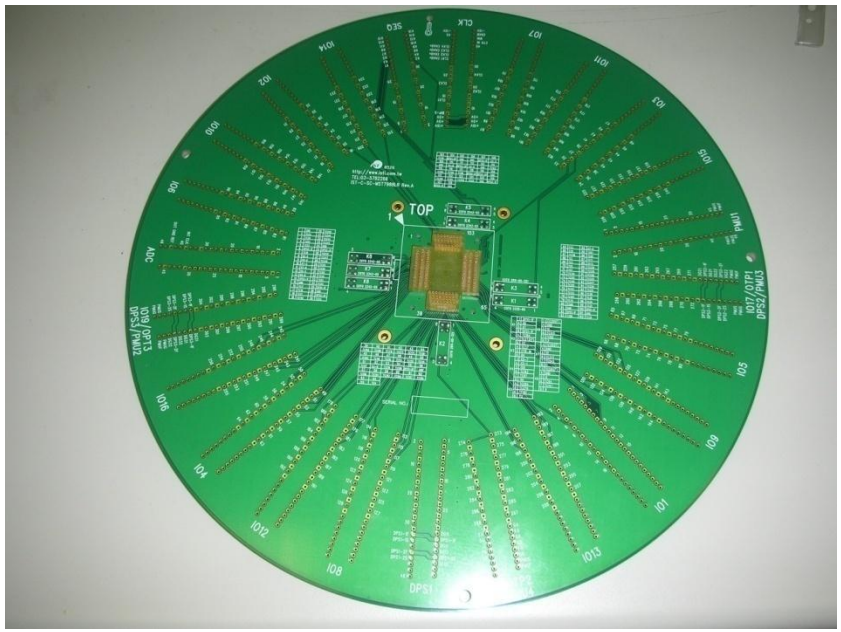


Prober

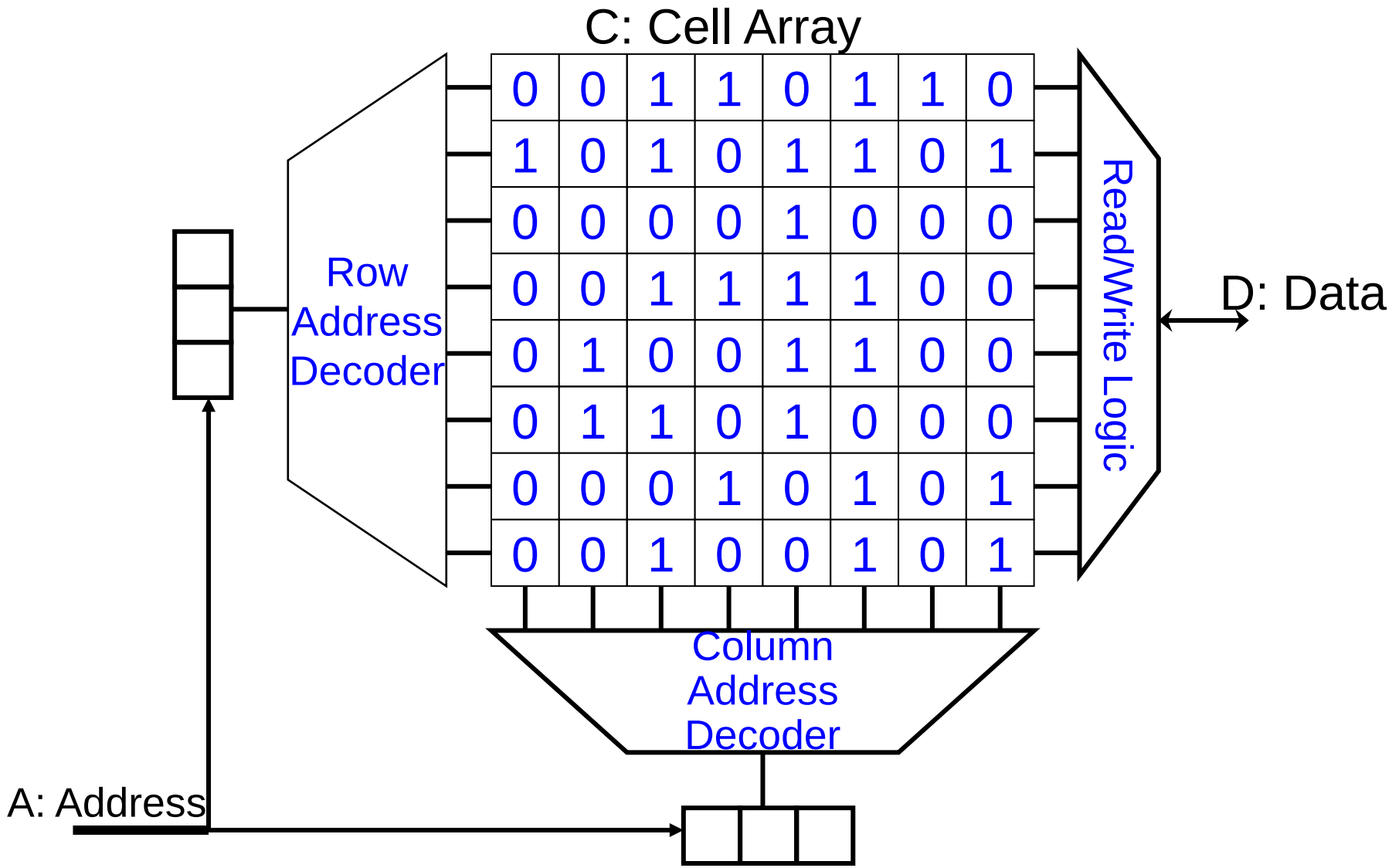
Final Test

Logic Tester

Load board

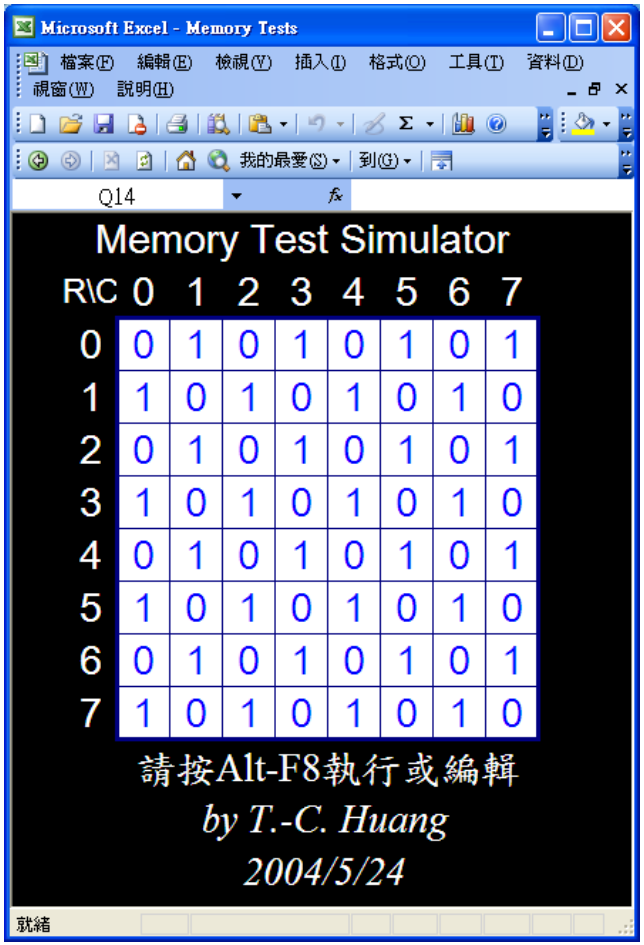


Typical Model of Memory Array



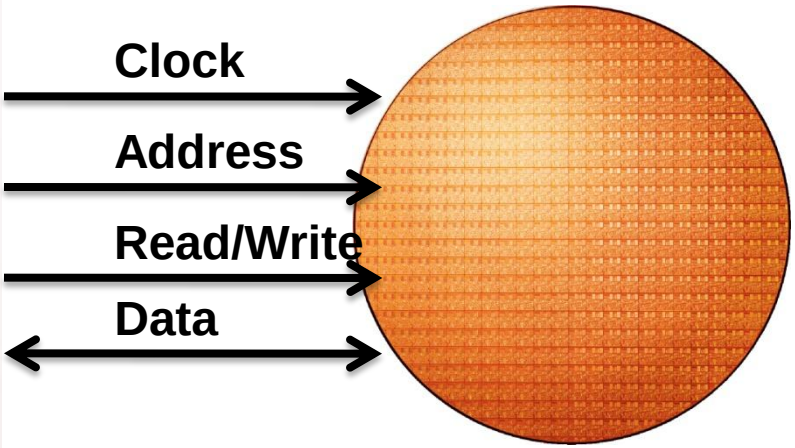
Brief Introduction to March Test

- Zero-One Algorithm
- Check-board Algorithm
- March C Algorithm
- Demo using an Excel file
- Usually we need multiple algorithms to promote the test coverage



Conventional Memory Test

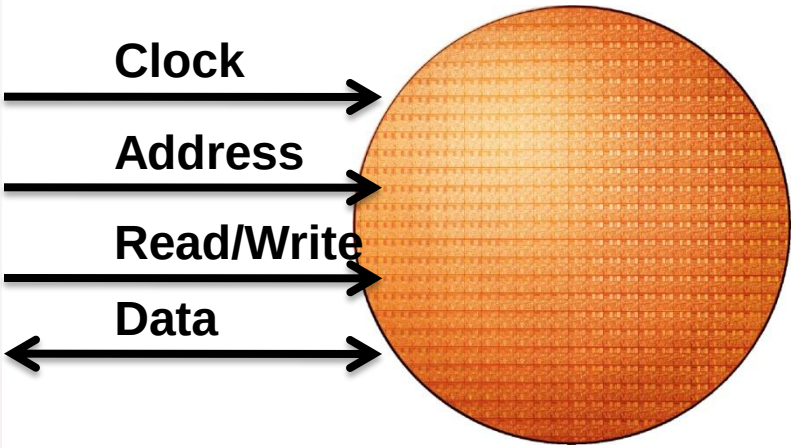
- External memory test
  - Typically 30M$/ATE ➔ Expensive!



Go/NoGo (Pass/Fail)

Conventional Memory Diagnosis

- External memory Diagnosis



Pros and Cons of MRAM

Pros and Cons of SST-MRAM Memory Switches	
Pros	**Cons**
Well defined physical Model and simulation tool. → Very fast improvement. Many chip level papers in IEDM, VLSI and ISSCC	MLC operation and stacking is difficult, although it was recently demonstrated.
No control device needed (for apple to apple comparison of STT-RAM vs. other ReRAM with control device)	Very much process dependent : ○ MgO dielectric Reliability (subsequent temp. and etching) ○ Thermal instability (< 150C), different from single cell results. ○ Even endurance as low as 1E7 (chip level) ○ H_c shift and stuck at 1 or 0 status (i.e. Narrow coercive window) ○ Variation
CMOS compatible and No High Voltages required - ease of front end integration.	All parameters are related to each other. Need to decouple (e.g. retention, programming current, RA, TMR, endurance, speed), (Keeping in mind memory device is simple.)
Extendibility : ~1-10μA Writing current @ 50ns speed (50nm diameter P-MTJ) (Even In-plane MTJ can be extendible)	Difficult to achieve production worthy process (many layers, process dependent, etc) complicated film structures: 10-12 different layers, deposited by PVD process for a thickness from ~8-20A and sputter etched.
More Scalable than PCRAM, Nanothermal and Nano electronic memory w.r.t write speed, endurance (>1E12) and retention.	High Read power, due to relatively low resistance
4F2 possible by vertical select transistor (Currently ~21F2, 40nm and chip level)	Still high programming or write current >100μA, cell size is limited by the driver device
MTJ can be extended to logic devices as a nonvolatile unit.	Concern about cross contamination if dedicated line is not allowed
Best suitable application ; Embedded, SRAM replacement, and SoC	High annealing temps required for high on/off (6:1) is incompatible with interconnect processing

Low Yield → Repair

Low Dependability → ECC

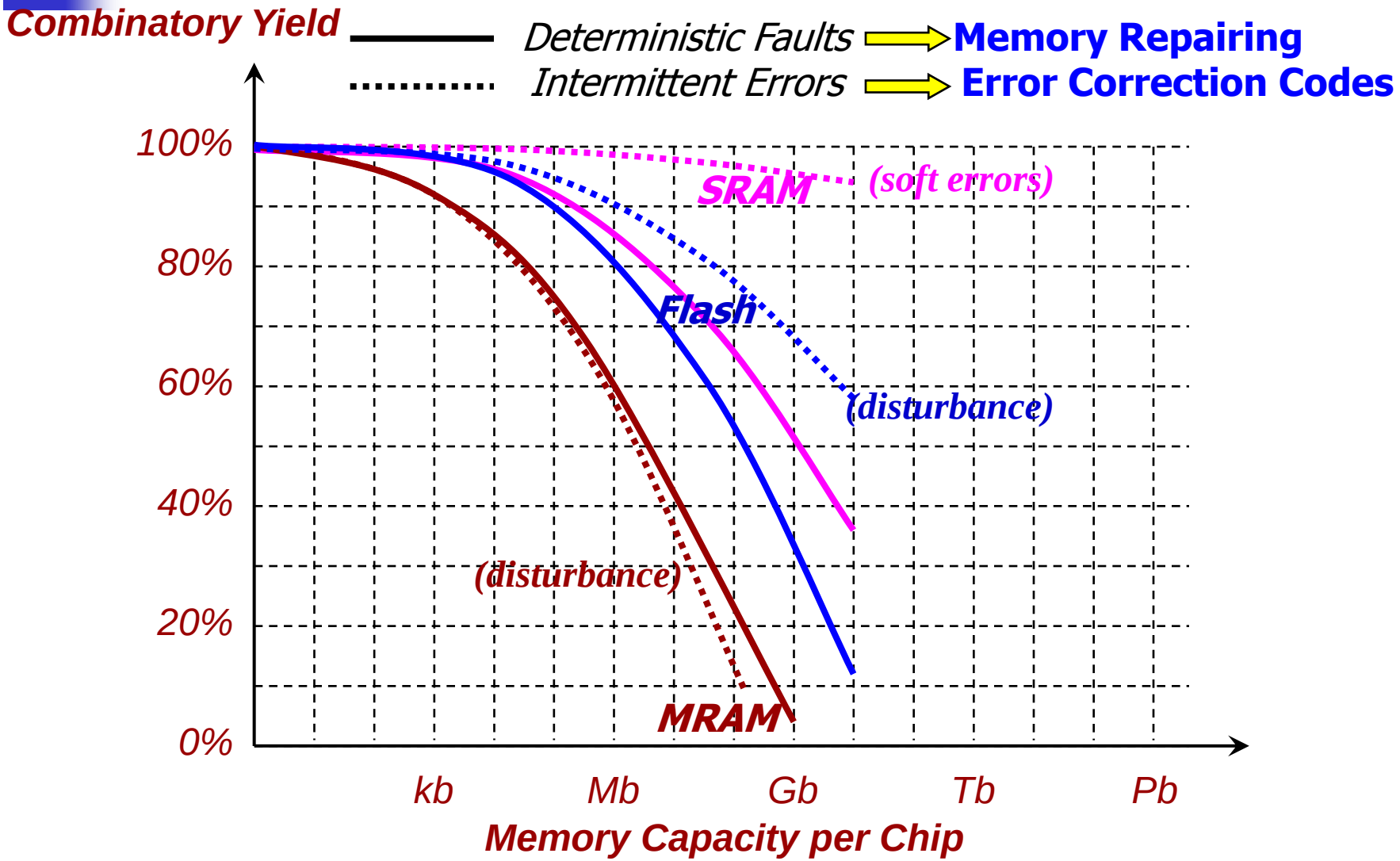
High R/W Current → Partitioned Power-Gating

SiP

3D-IC

(Source: ITRS2010)

Yield and Dependability



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Fault Models

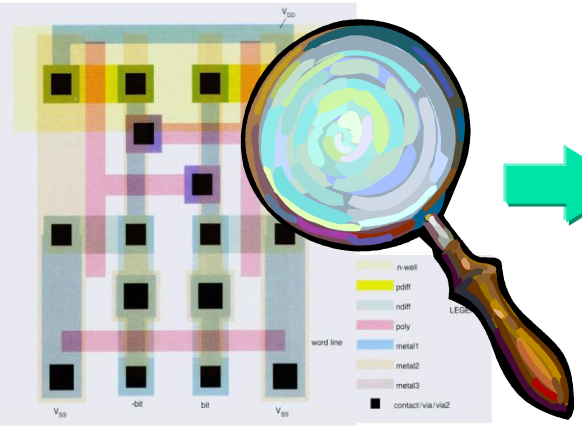
- Fault (Type) Model
  - Stuck-At Faults
  - Coupling Faults
  - Neighborhood-Pattern Sensitive Faults
  - Transition Faults
  - Retention Faults
- Fault Distributing Model
  - Line Faults
    - ✓ Row, Column
    - ✓ Clustered Faults
    - ✓ What else? ➔ Hypercube Faults ??

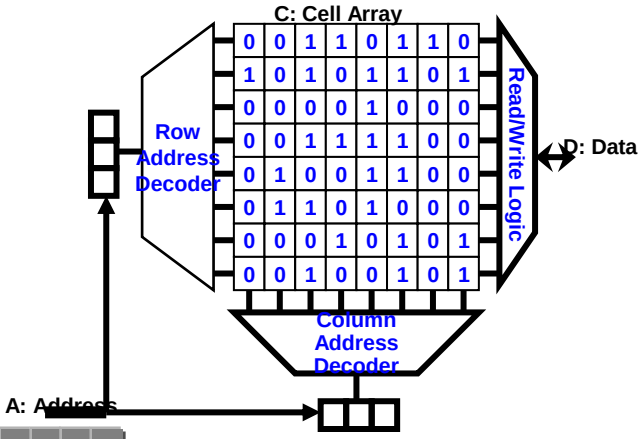
More Serious for MRAM

Fault Distribution Model

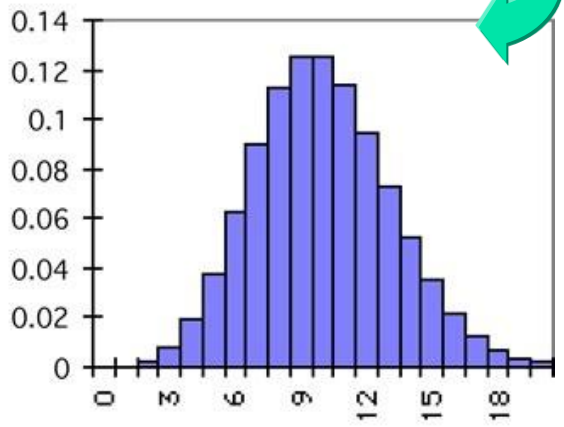
IFA (*Inductive Fault Analysis*)

Fault Models Massive Diagnoses

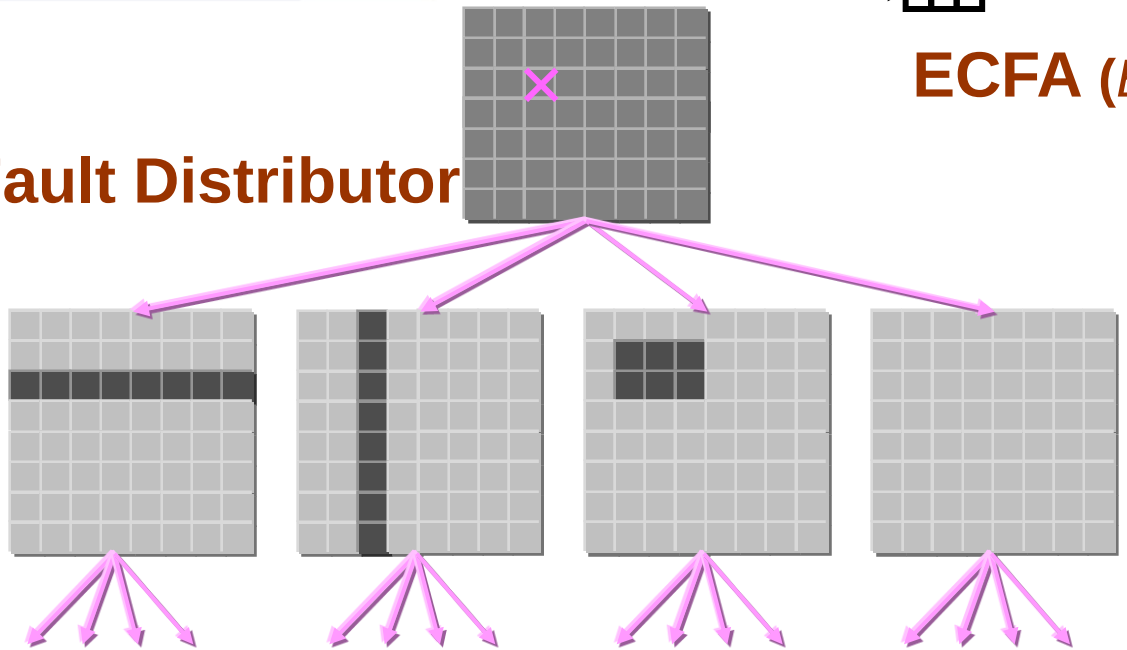




ECFA (*Effect-Cause Fault Analysis*)

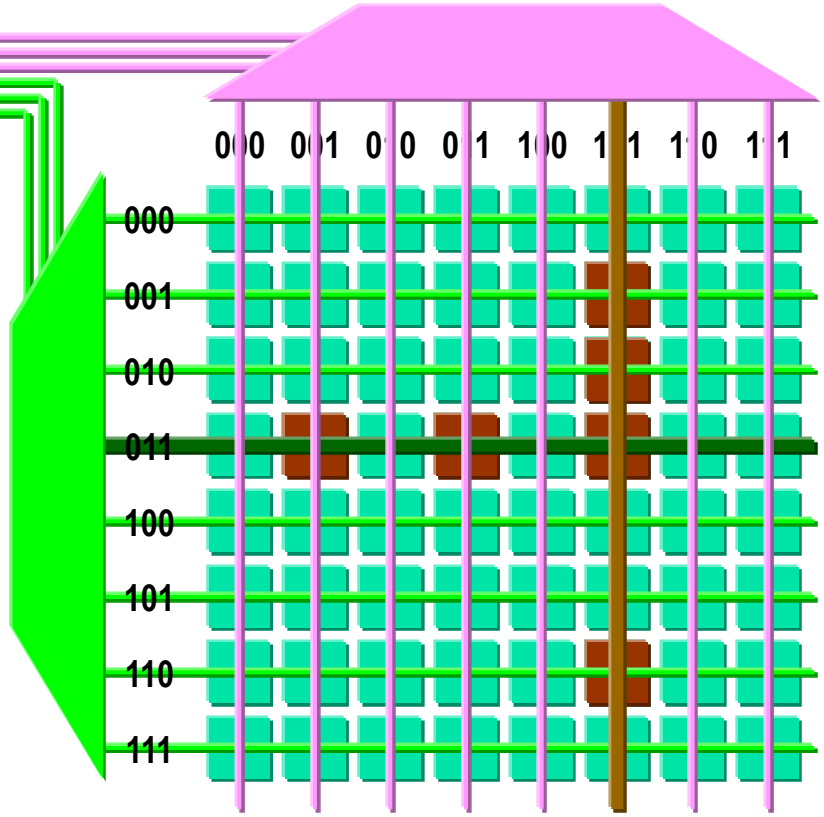


Fault Distributor



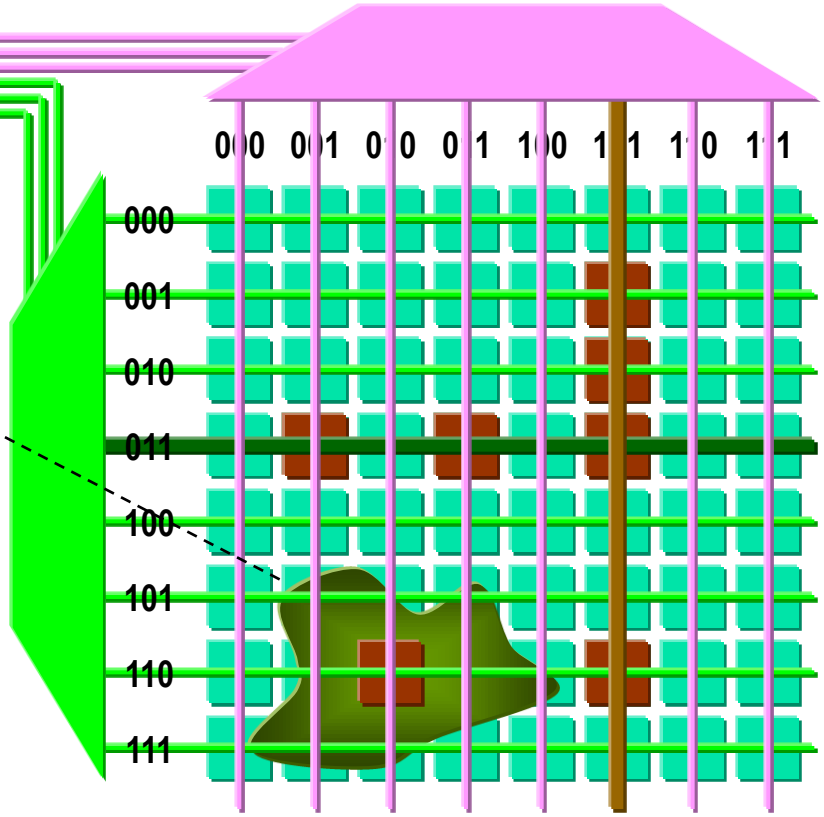
Early Distribution Models

- Fault Types:
  - Uniformly Random Faults
  - Line Faults
    - ✓Word-Line (Row)
    - ✓Bit-Line (Column)
- Some Previous Work:
  - CRESTA, 2000 [6]
  - BRAVES, 2003 [3]
  - Fault Distributor, 2007 [13]



Recent Distribution Models

- Additional Fault Type:
  - + Clustered Faults
- Major Previous Work:
  - MESP/Divided-Lines, 2010 [11]



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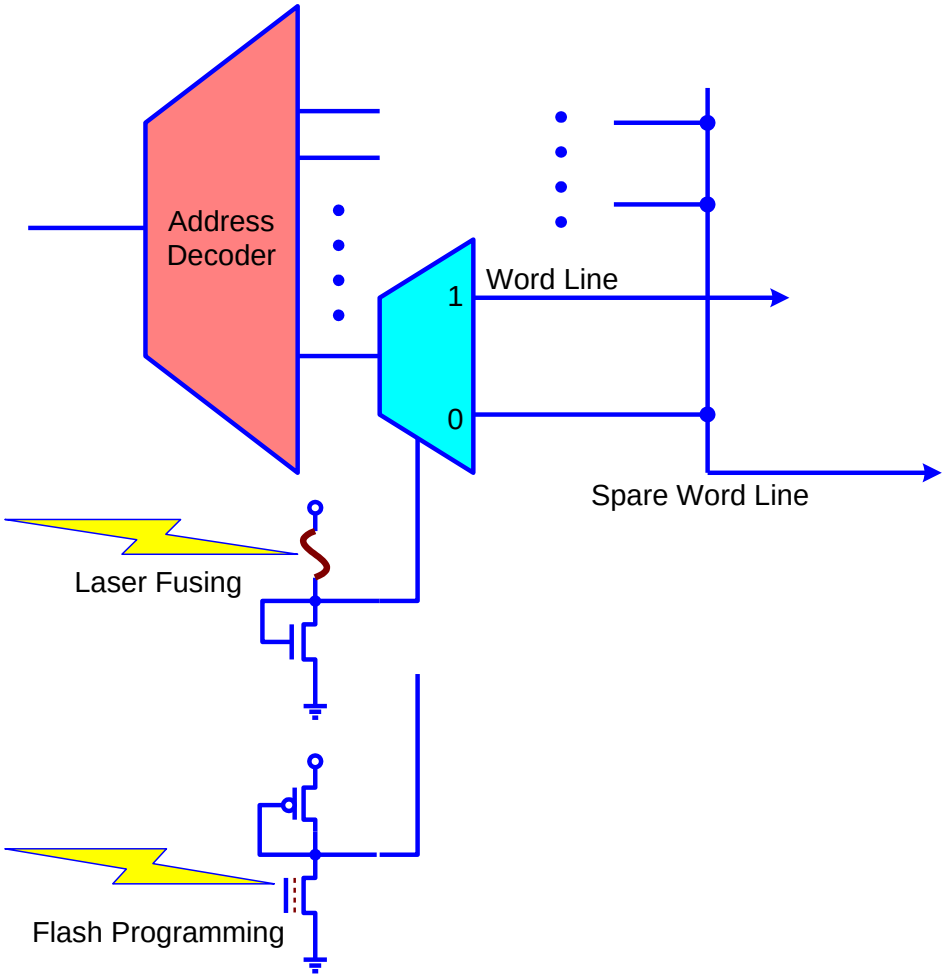
Conventional Memory Repair

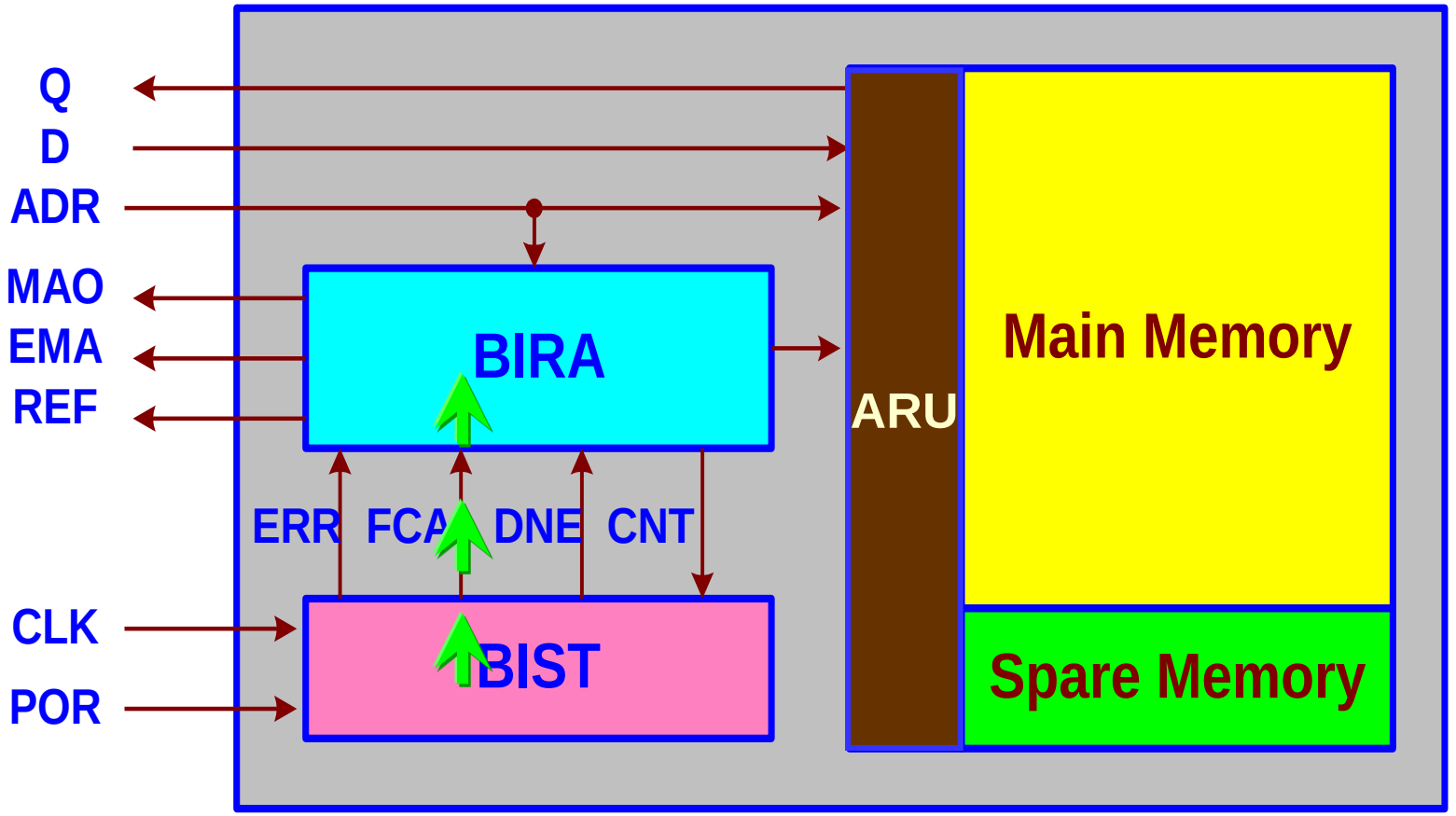
- Laser Fusing or Flash Programming

(Source: GSI Group)

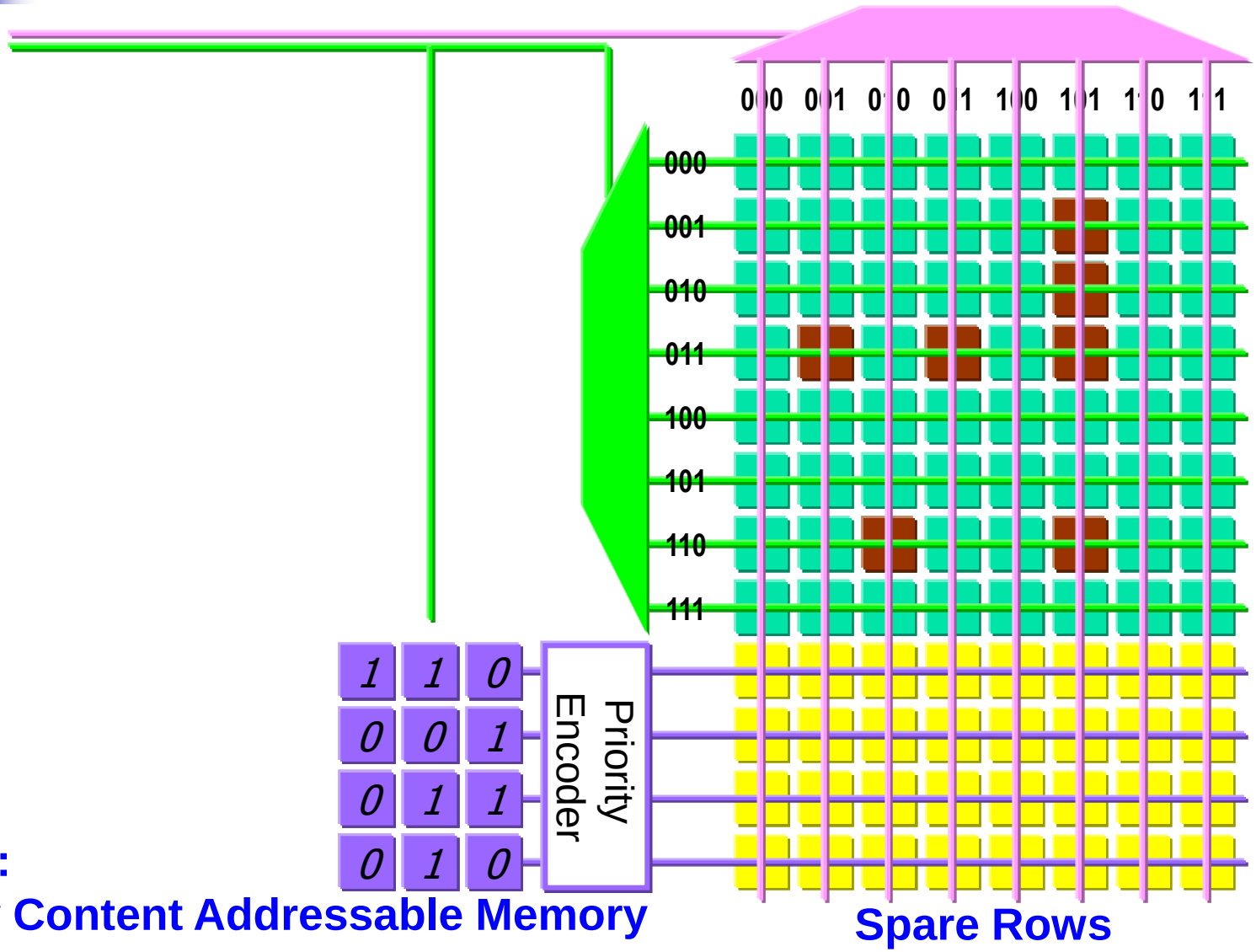


BISR: Built-In Self-Repair

- A typical BISR scheme

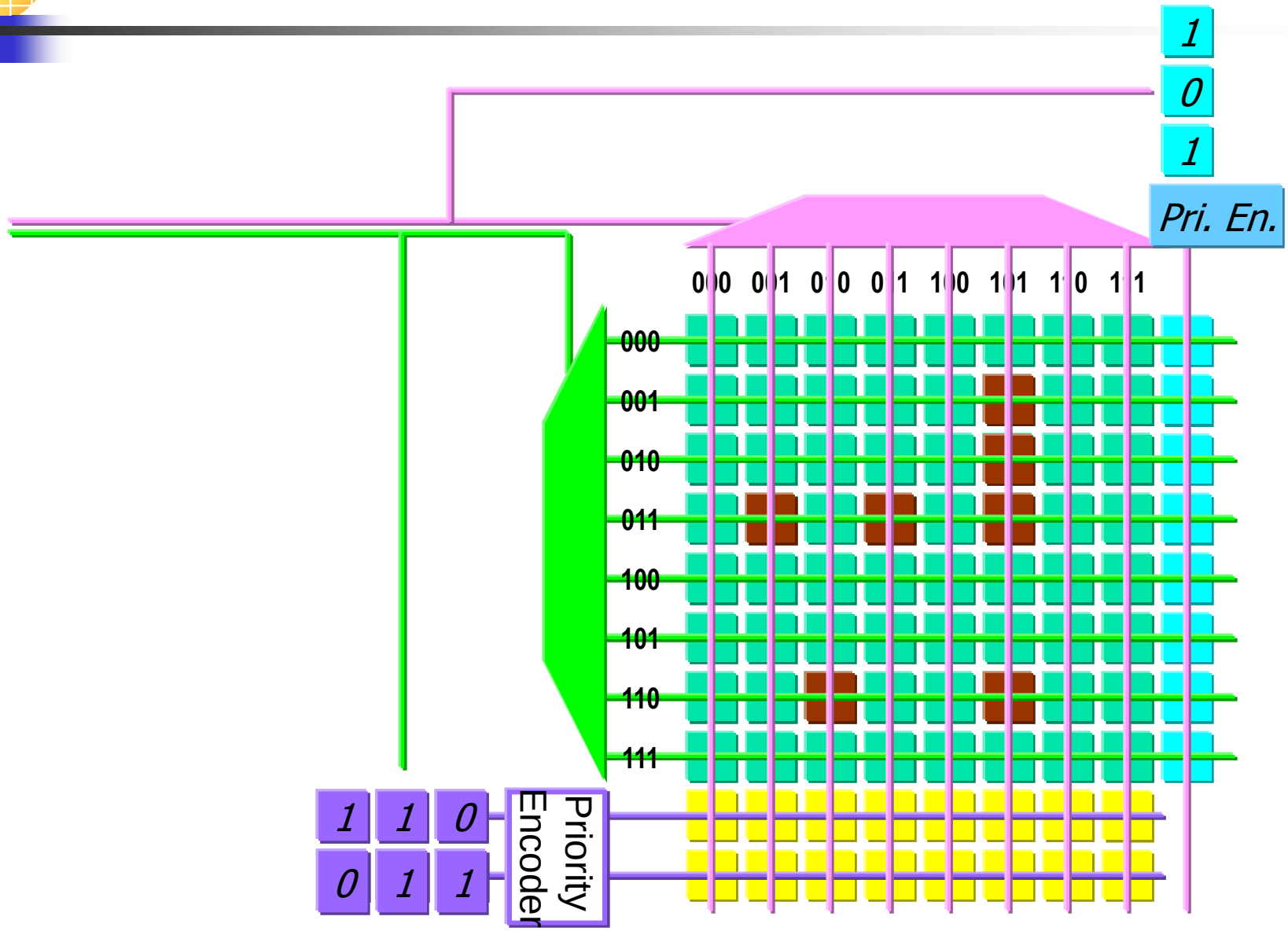


BISR with Spare Rows



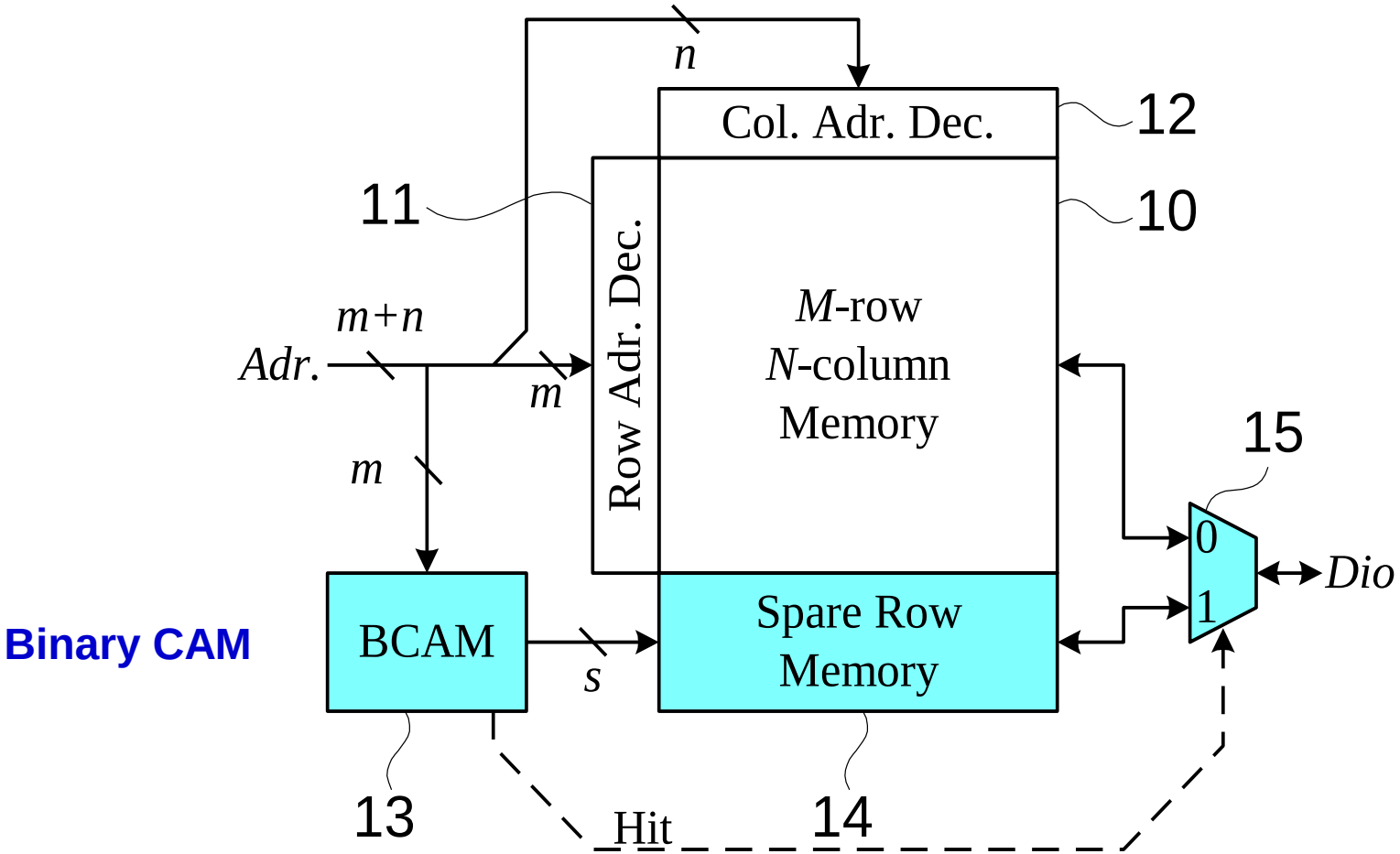
BCAM:
Binary Content Addressable Memory

Spare Rows and Columns



Conventional Memory Repair

BCAM-based Remap



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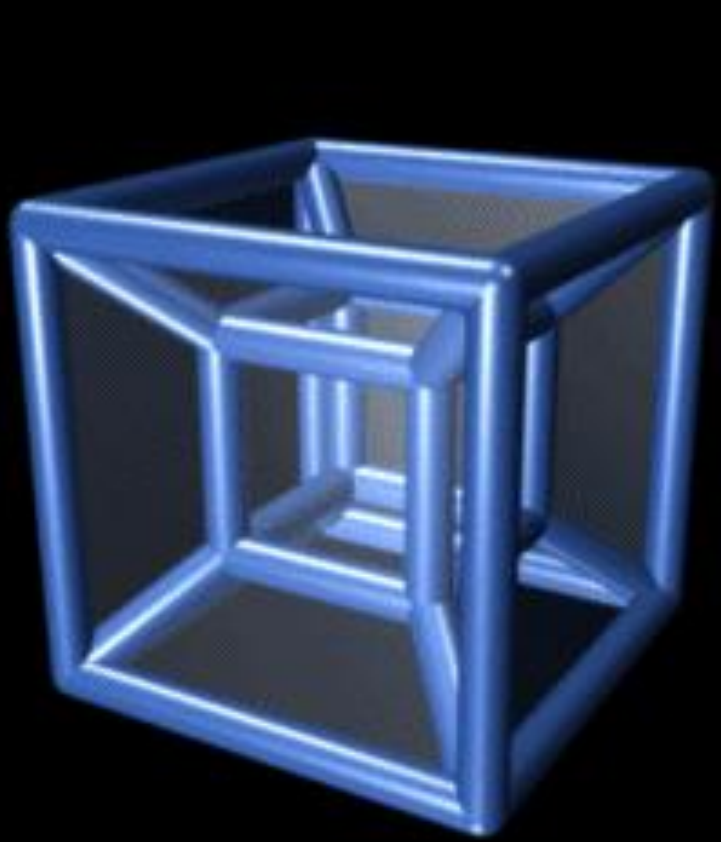
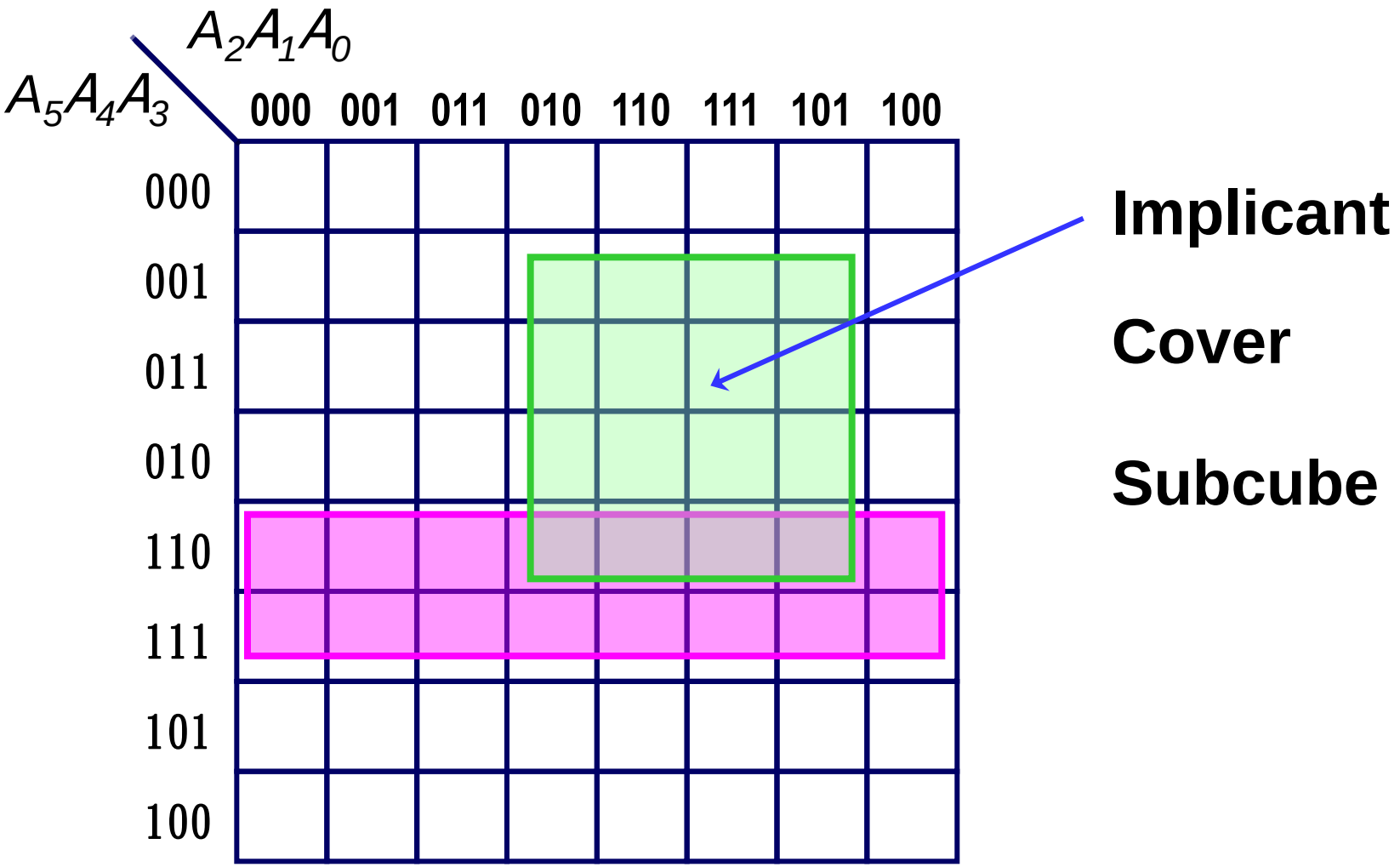
Hypercubes: Two 4-Cubes



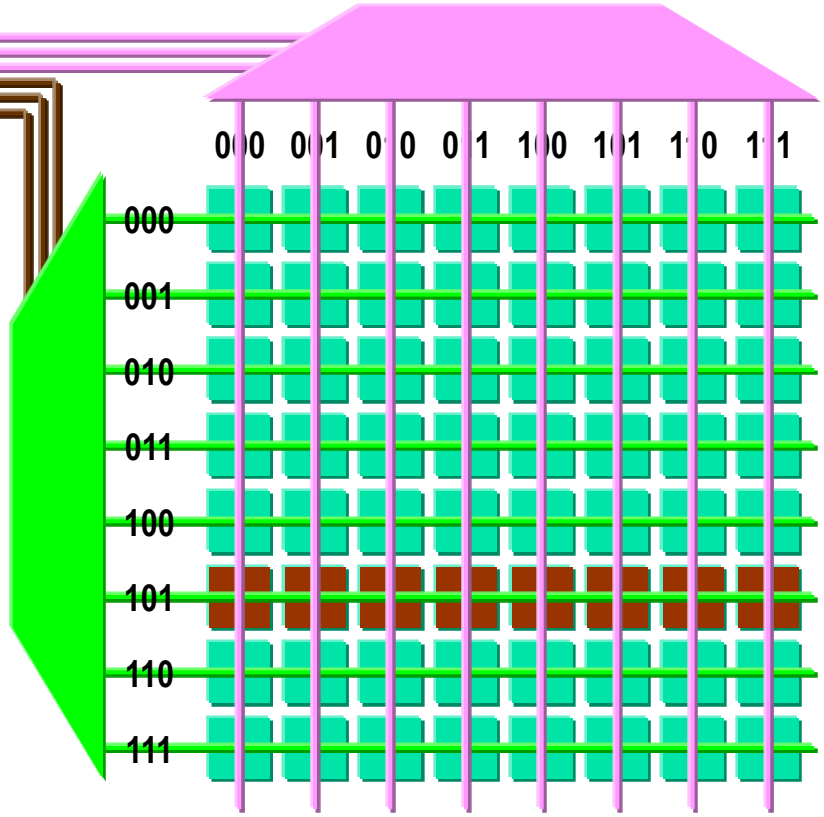
(Figures released from Google)

K-Map representing a Hypercube



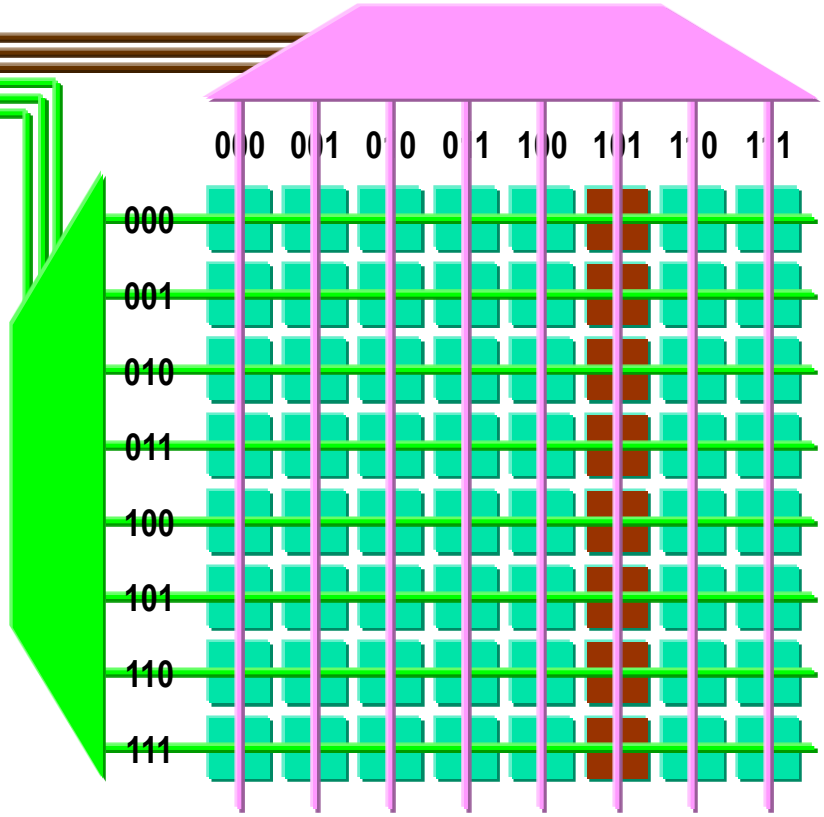
More Multi-Fault Occurrence

- Address Line Faults
  - Row



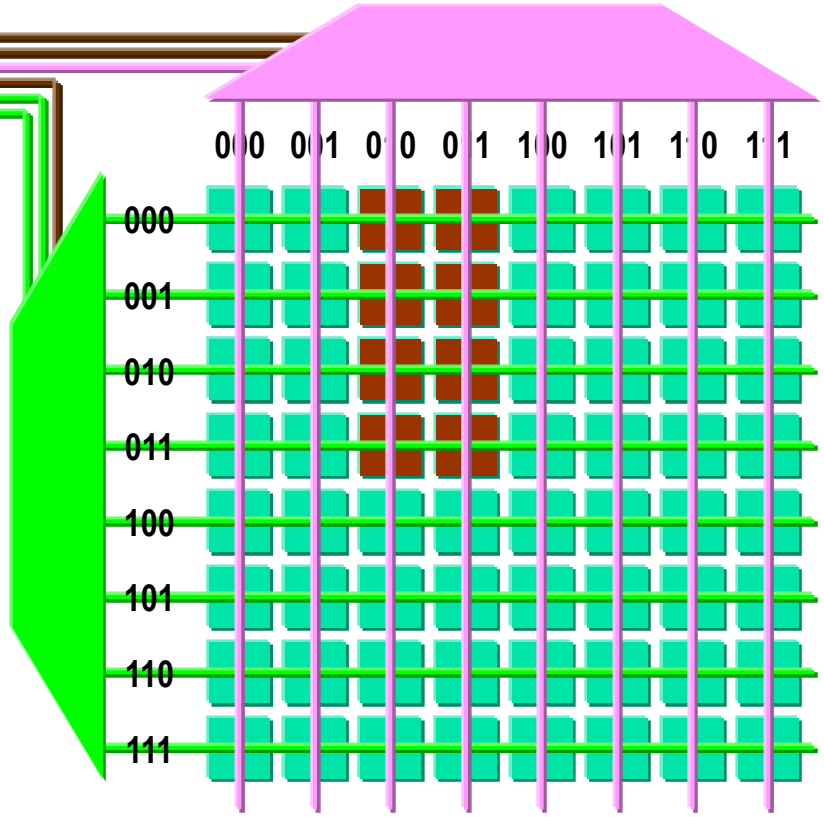
More Multi-Fault Occurrence

- Address Line Faults
  - Column



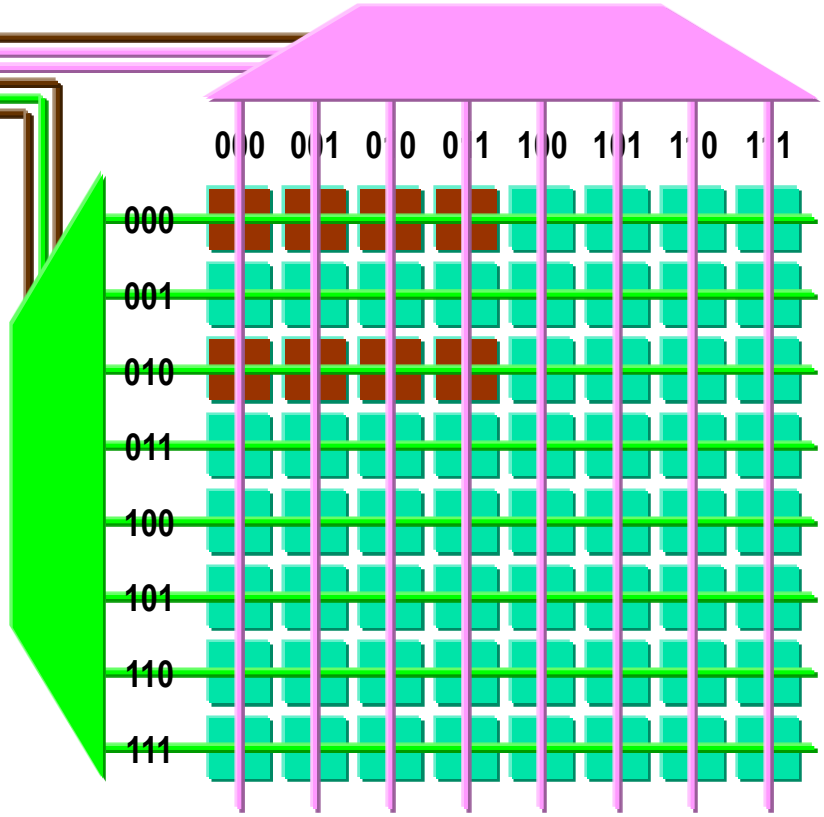
More Multi-Fault Occurrence

- Address Line Faults
  - Cluster



More Multi-Fault Occurrence

- Address Line Faults
  - Scattered Clusters probably due to address fluctuation



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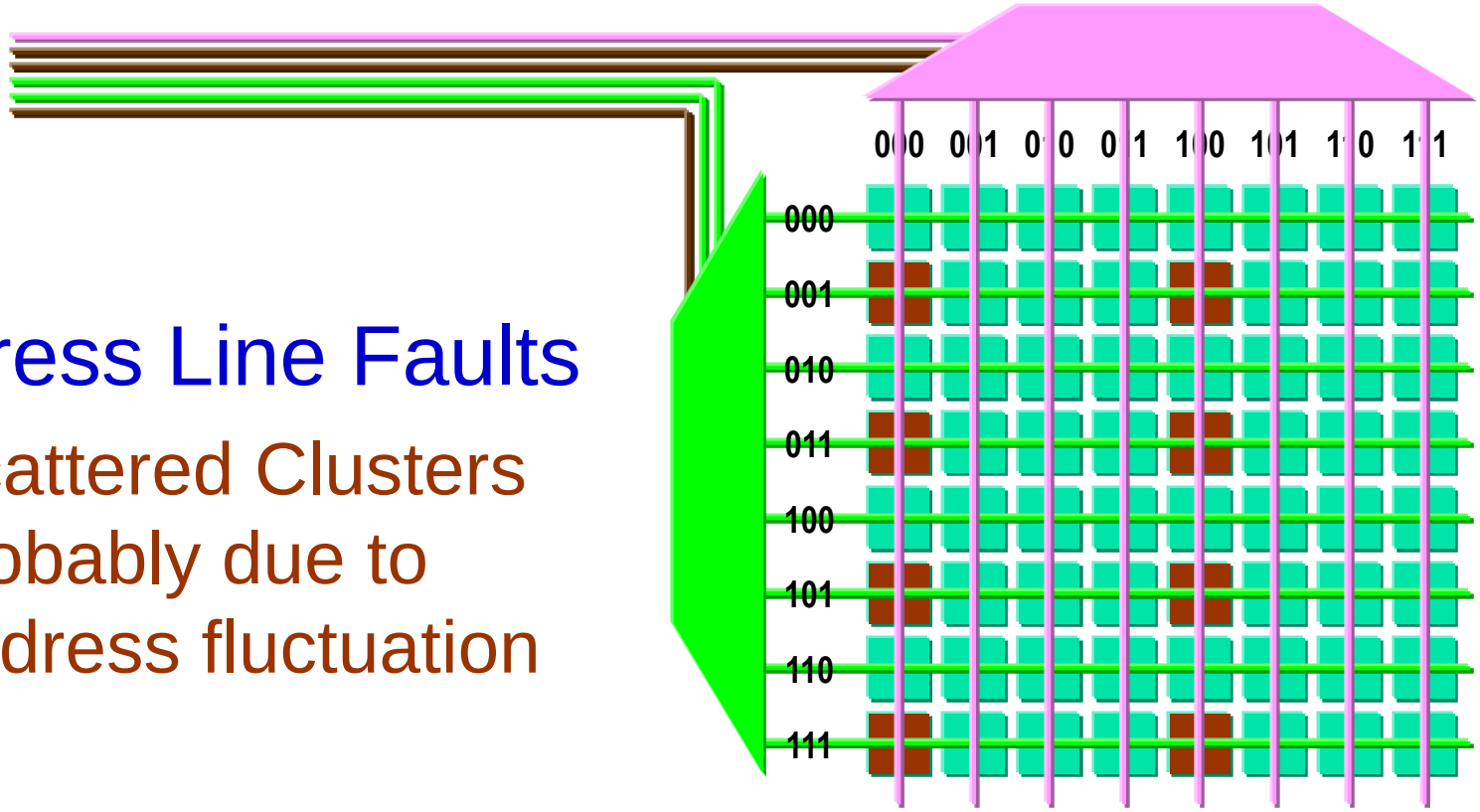
- Address Line Faults
  - Scattered Clusters probably due to address fluctuation



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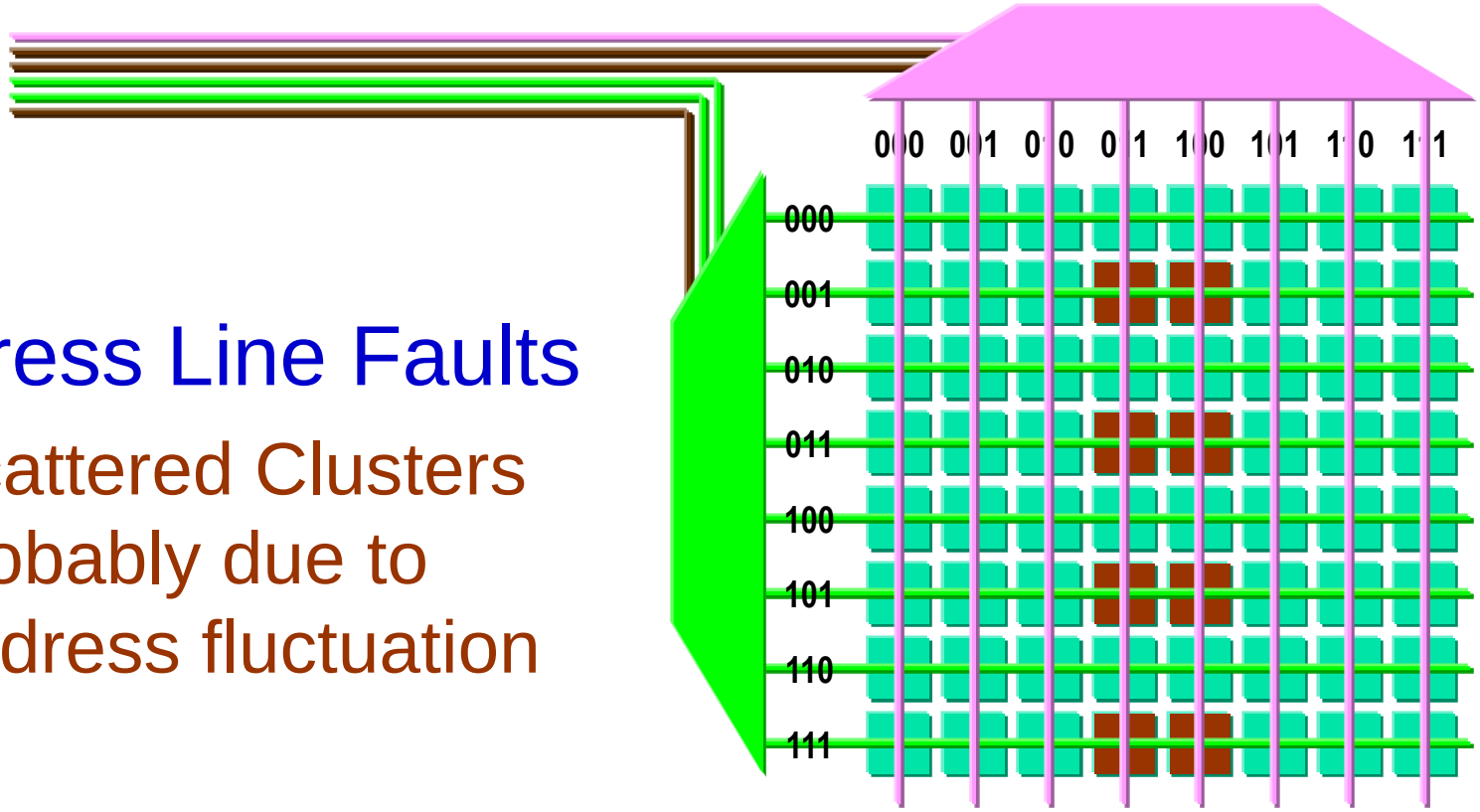

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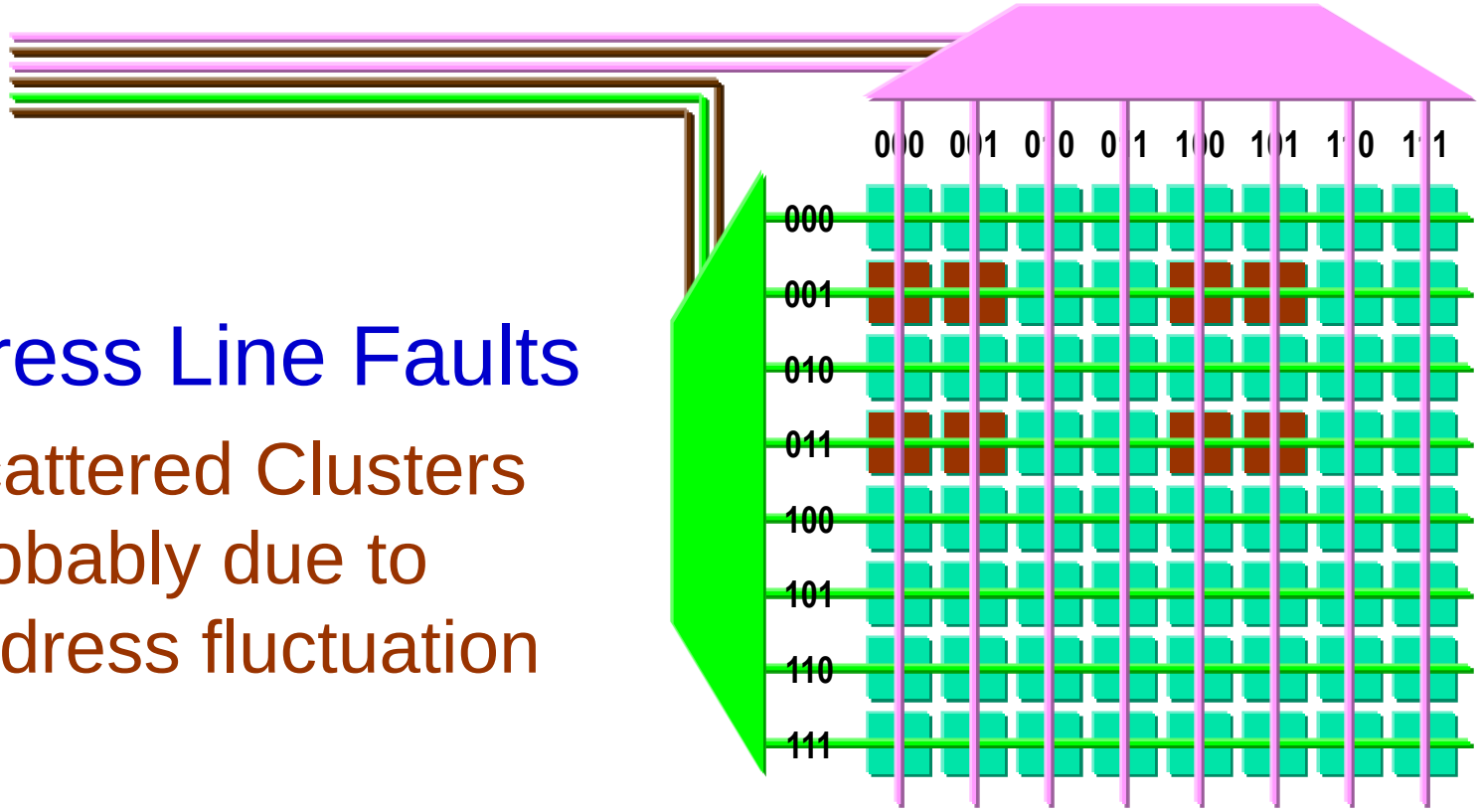

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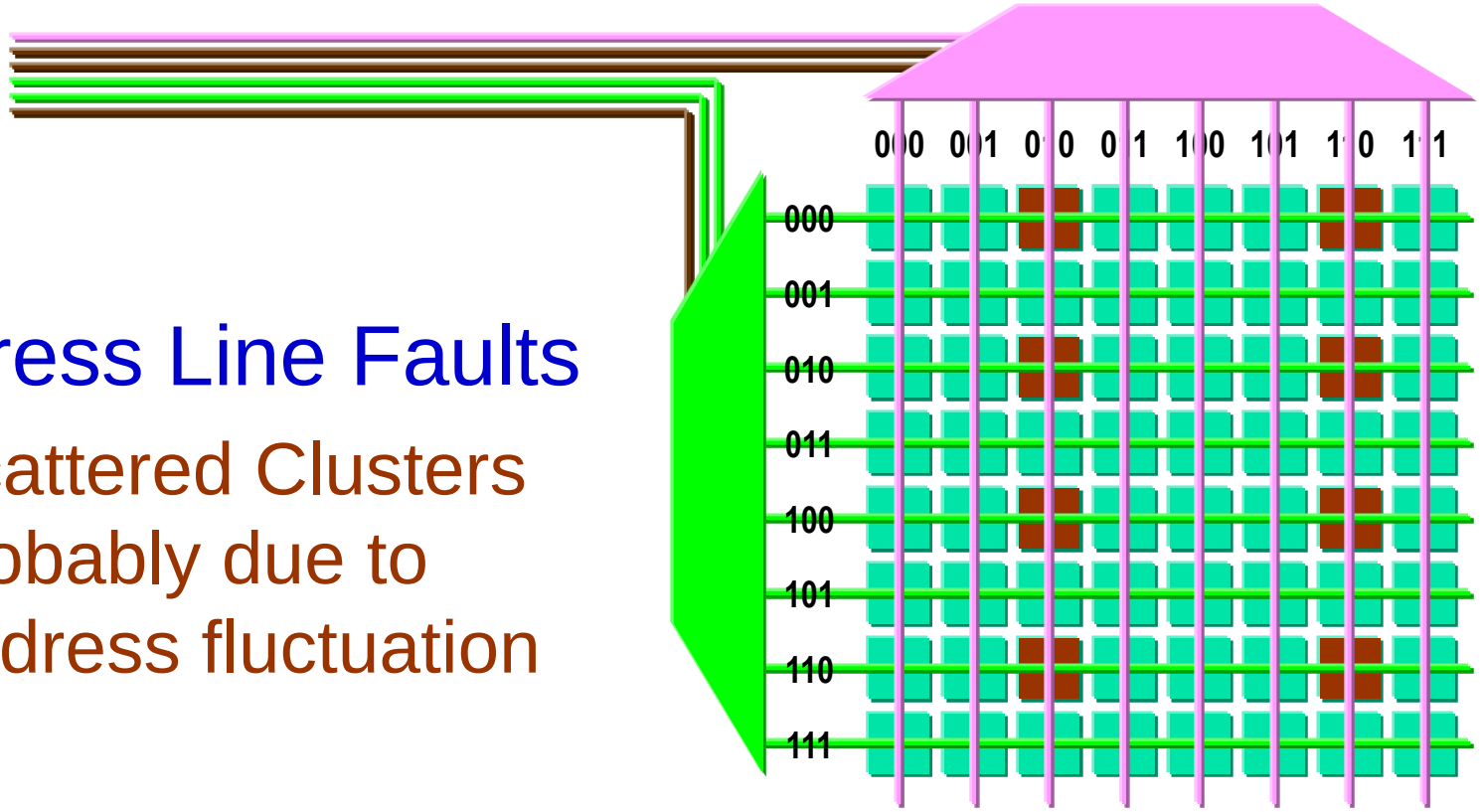
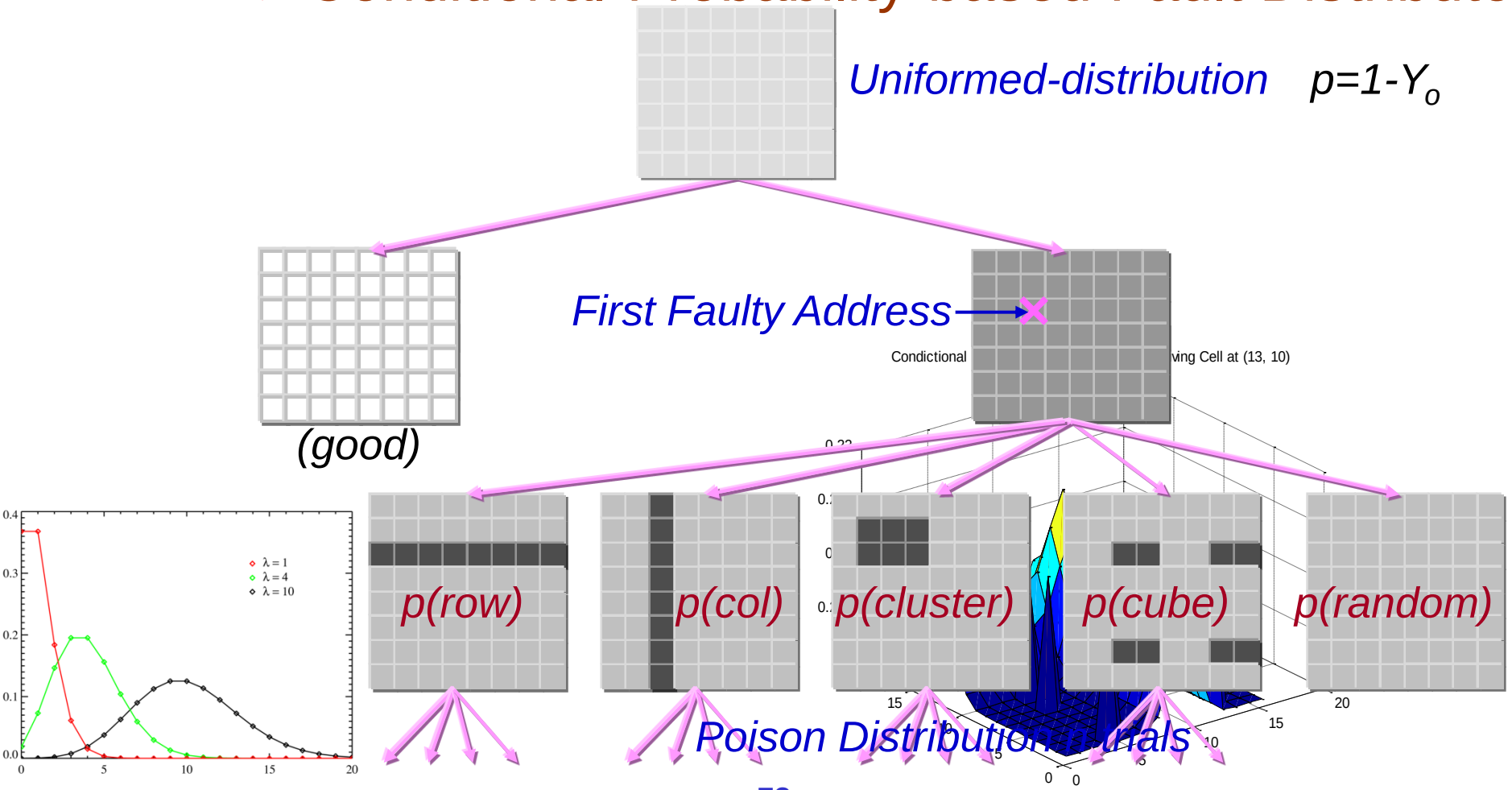


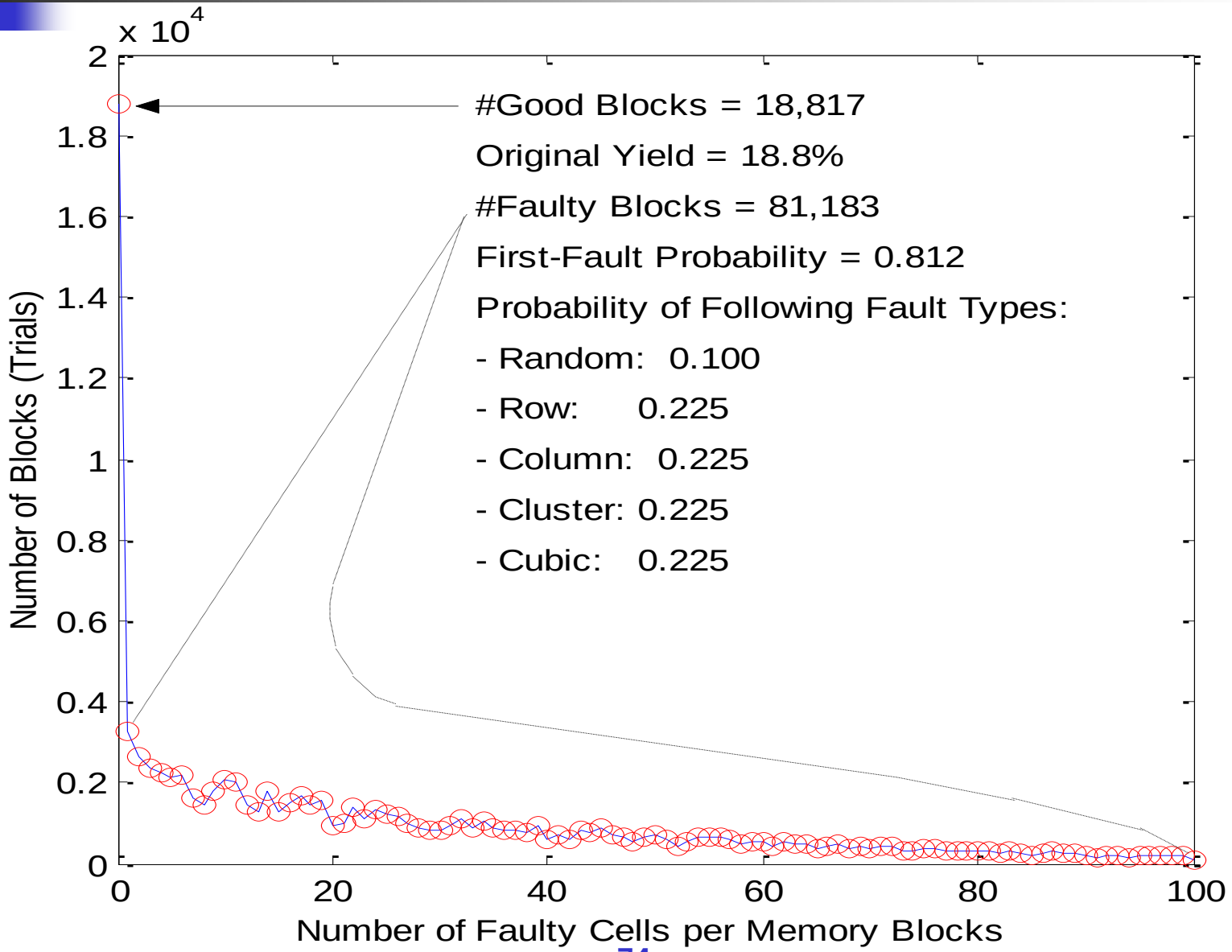
Proposed VERA

Verifier/Estimator *for Redundancy Analysis*

Conditional-Probability-based Fault Distributor



Result Histogram



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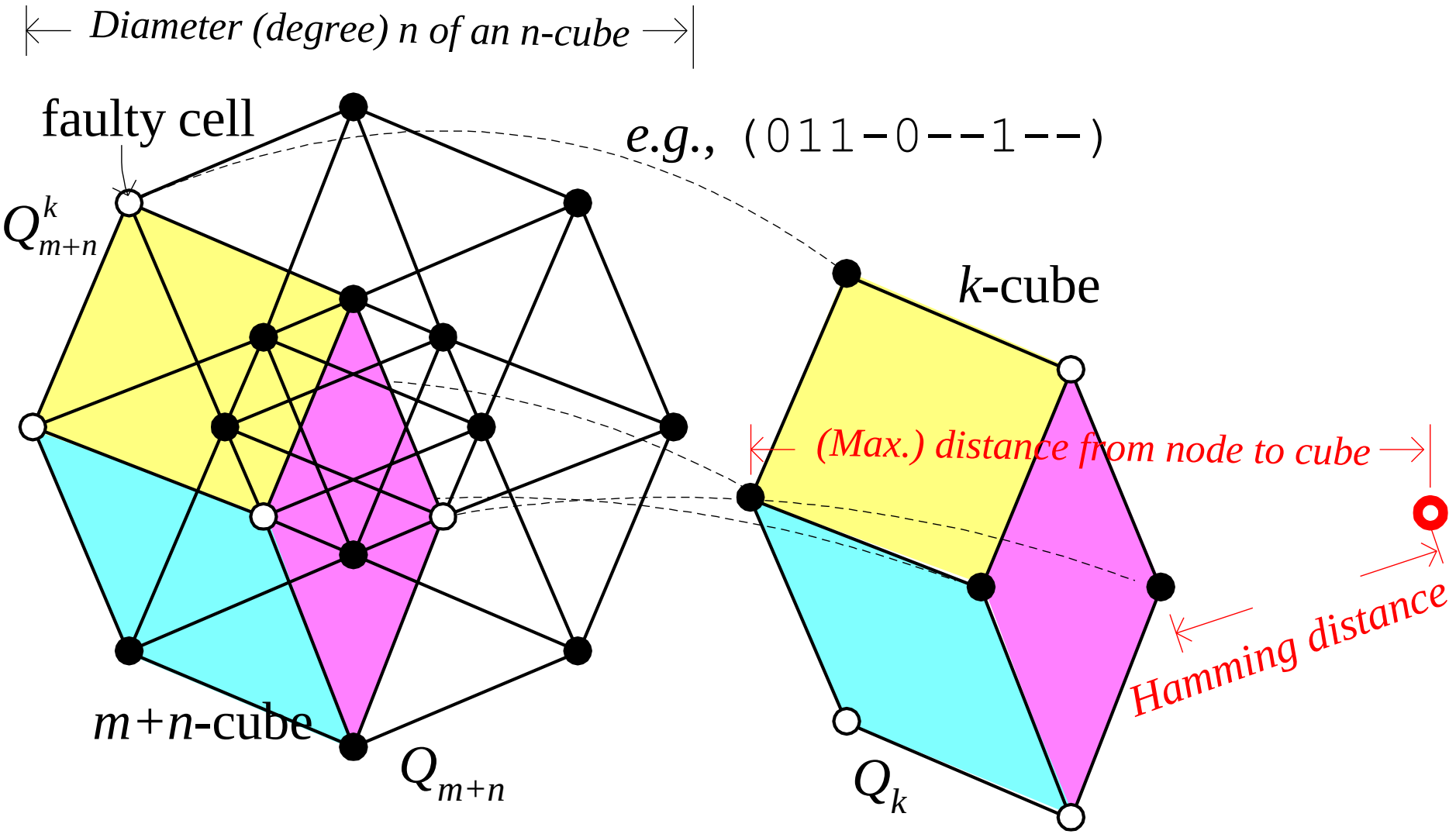
Basic Concept



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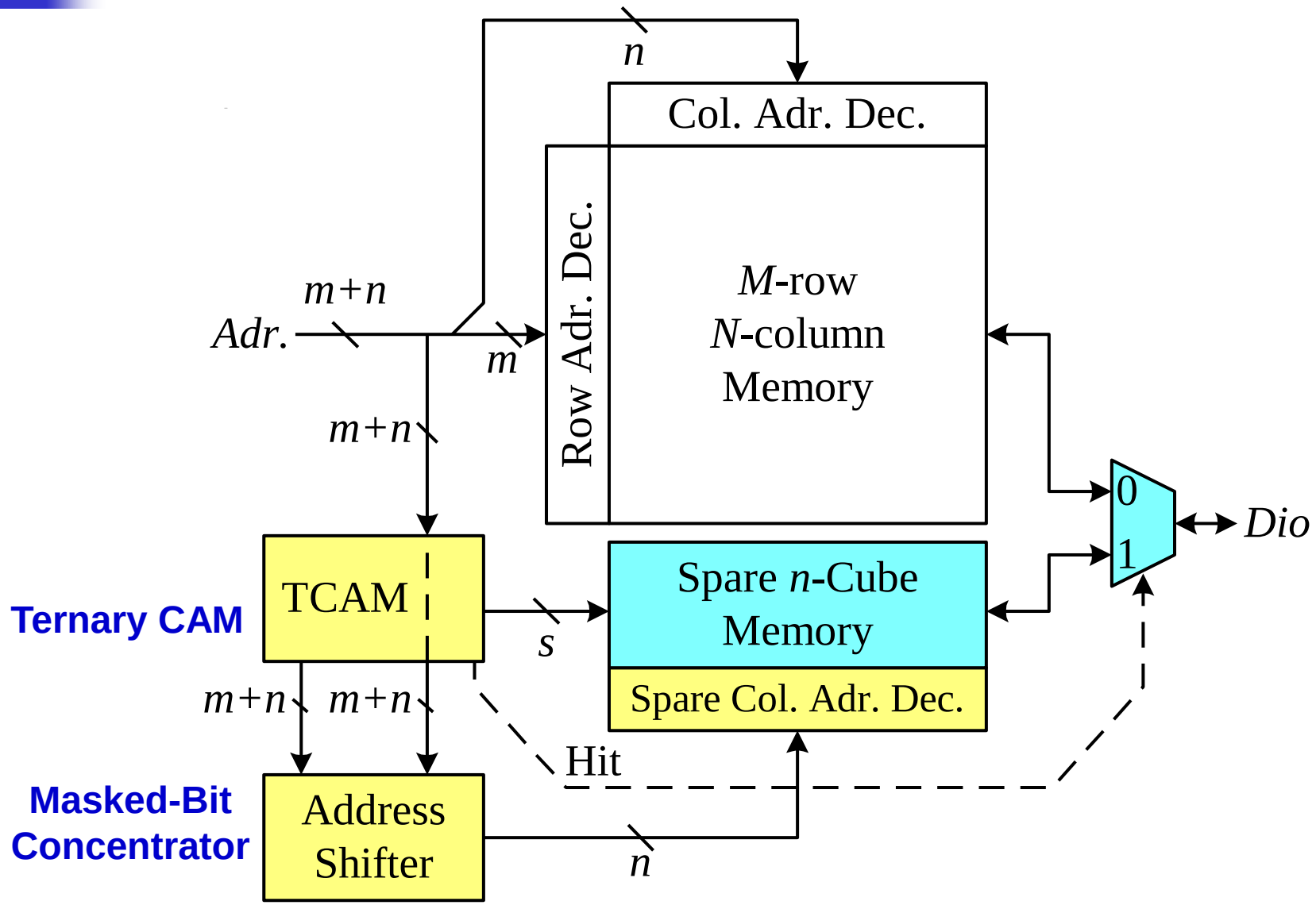
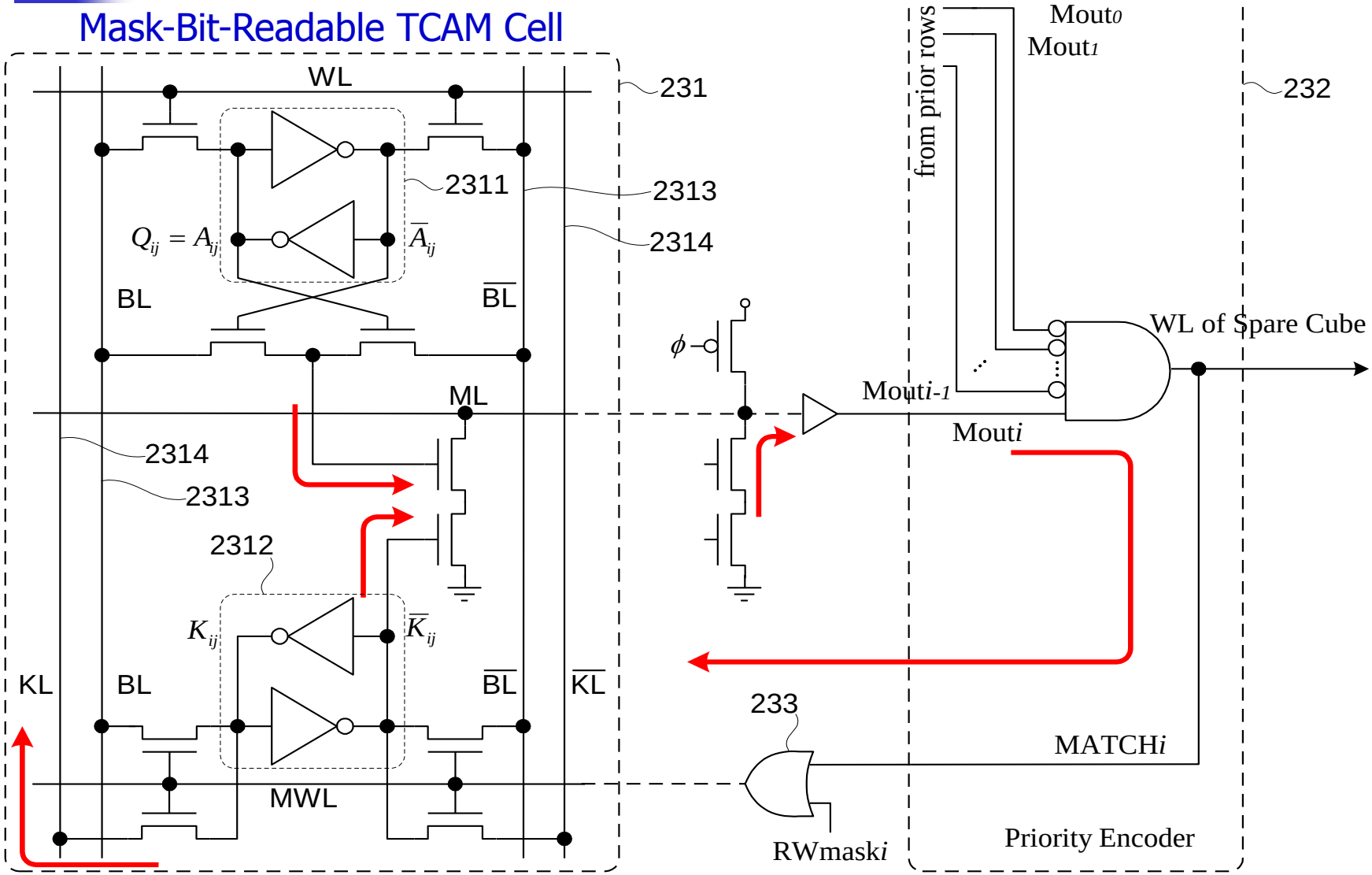
Hypercube-based Remapping

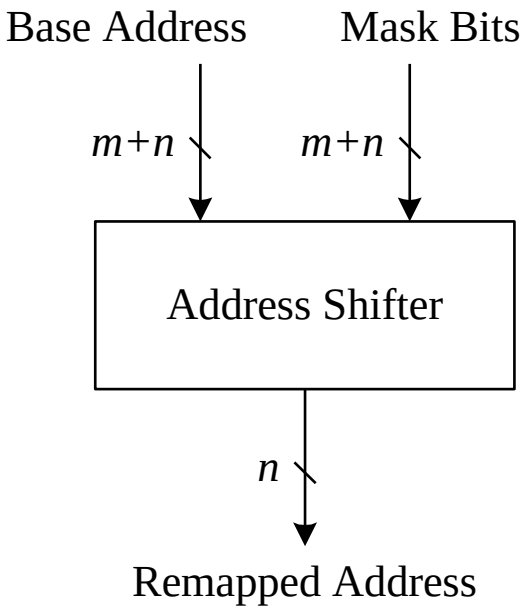


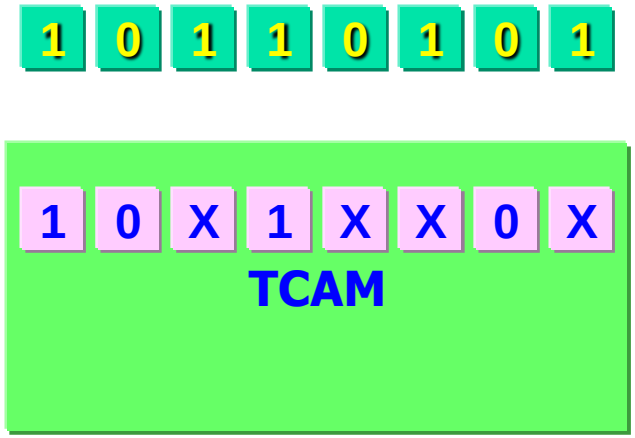
Proposed TCAM Design



Address (Bubble) Shifter

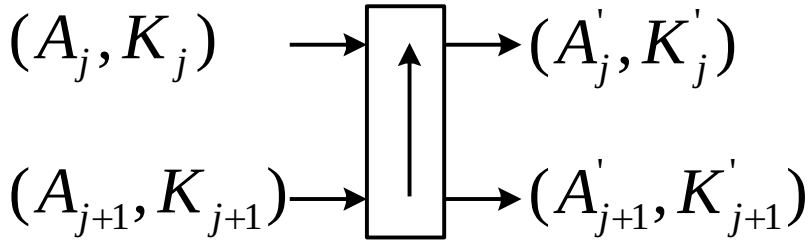
- If matched by the TCAM comparison
  - Extract the masked address bits to a sub-address
  - Also called “Masked Bit Concentrator”
  - Not necessarily in order but bijective (1-1)



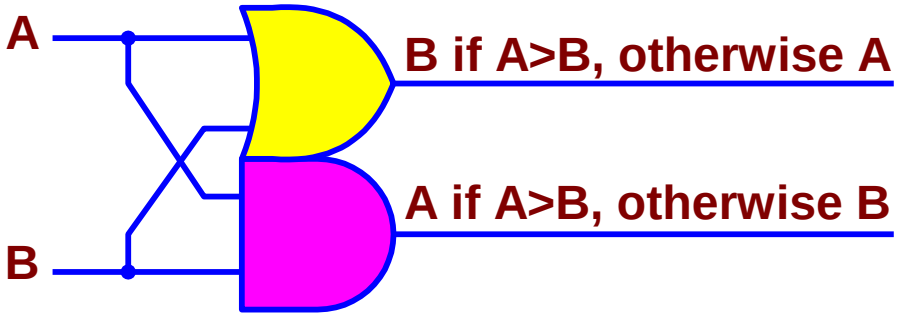


Swapper in the Address Shifter

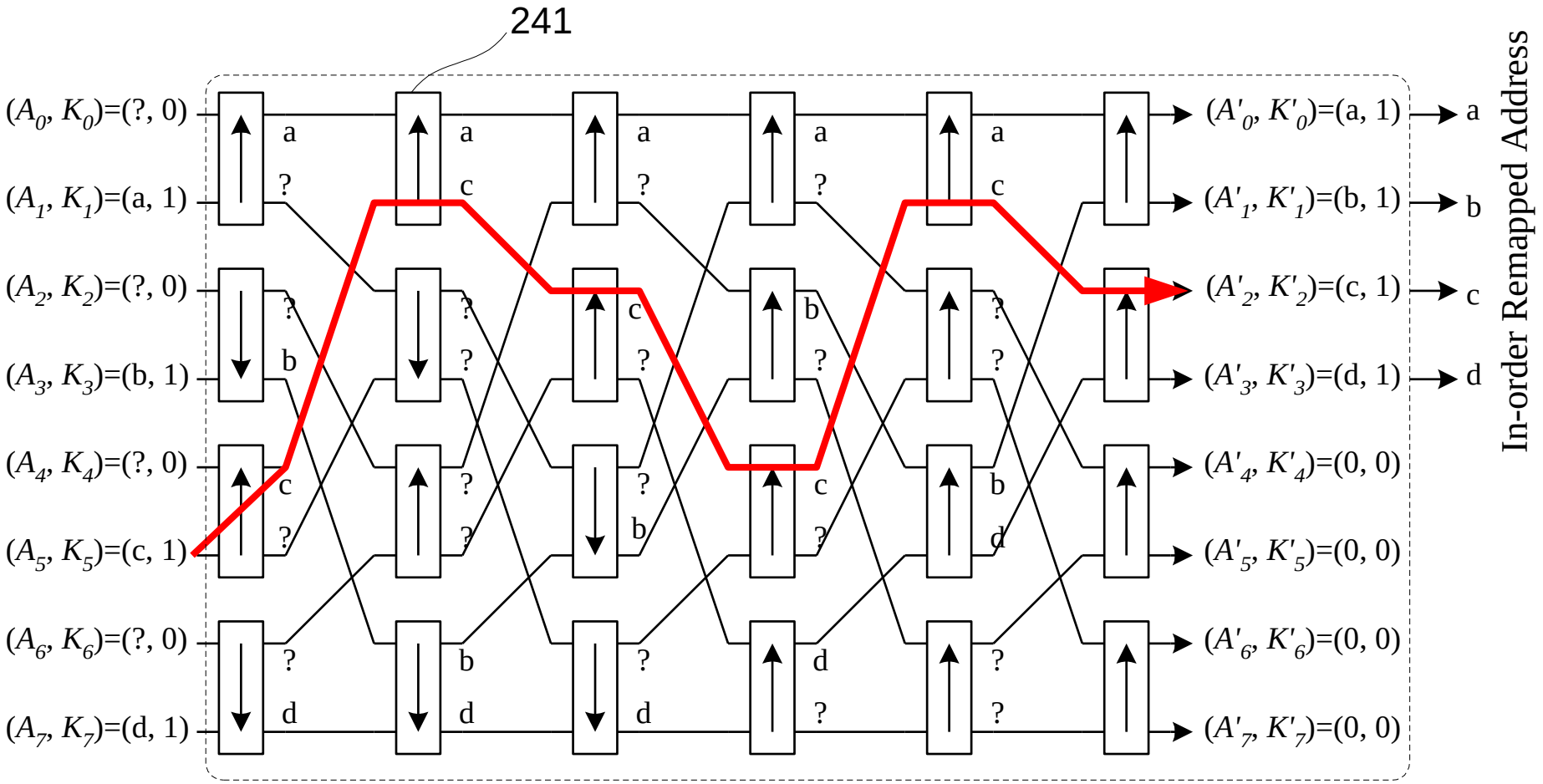
- Swapper in Binary Sorting Network



- Only 1 Level of CMOS gates for 1 Stage

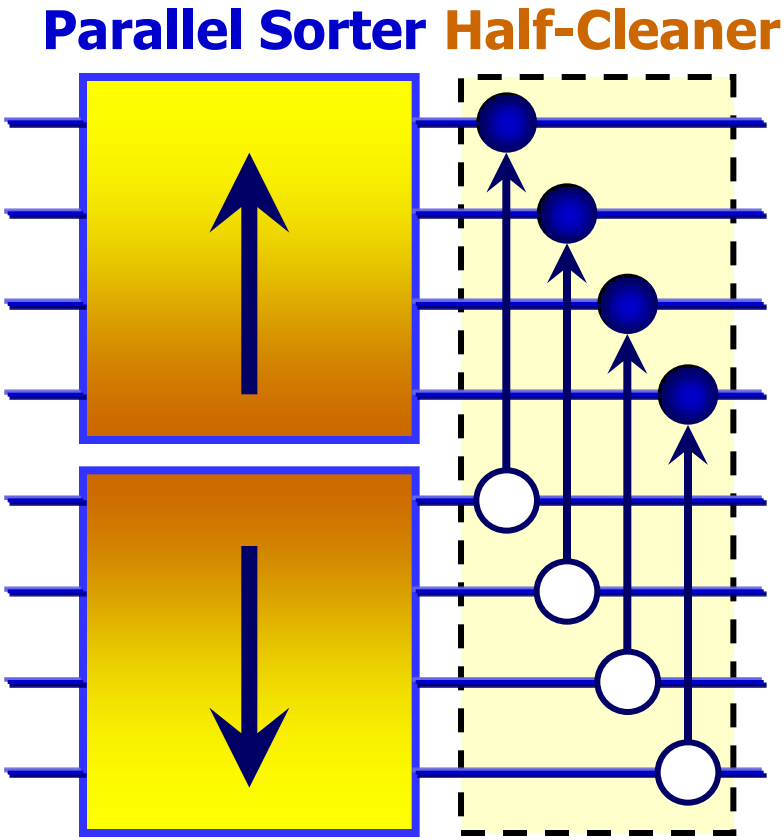


Address Shifter using a Parallel Sorter($2n$)



- Extracting the sub-address IN ORDER.

Address Shifter using a Bitonic Sorter



#inputs N	n $=log_2$ N	Parallel Sorter	New Concen-trator	%Red. (Area) (Time)
4	2	3	2	33
8	3	6	4	33
16	4	10	7	30
32	5	15	11	27

- Extracting the sub-address IN BIJECTION.

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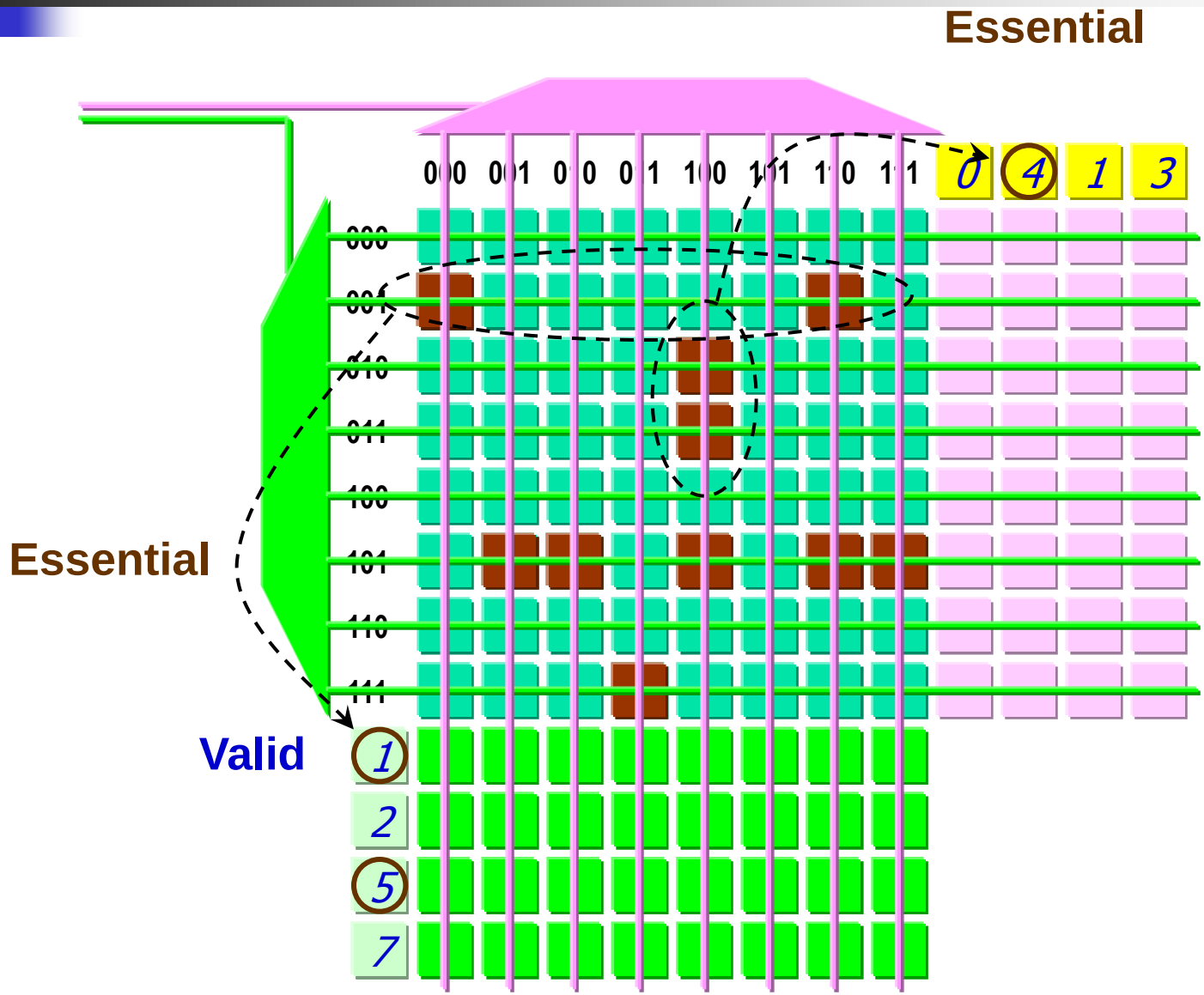
Eg. Essential Spare Pivoting [3]



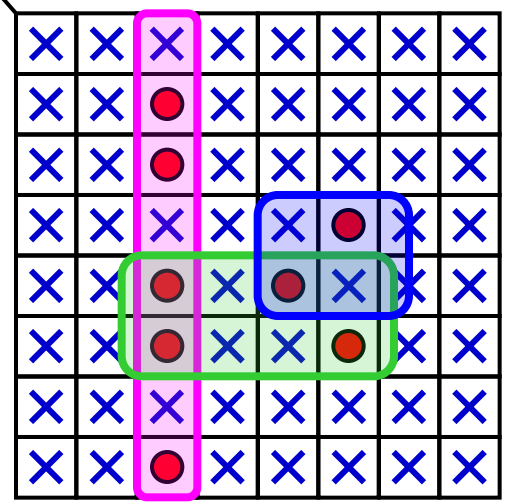
HYPERA (Redundancy Analysis)

- Modified Quine-McCluskey Algorithm
  - Externally Repairing
  - Repair-Rate Optimized
- Essential Cube Pivoting Algorithm
  - Modified from Essential Spare Pivoting Algorithm for Hypercube-based Architecture
  - Reduce the BIRA Complexity in a greedy manner.

Modified QMA *for External Analysis*

1. *Let the maximum degree of spare subcubes be n. Initialize all faulty cell addresses as subcubes of degree* $d_1 = 0$.
2. *Sort all subcubes of degree* d_1 *by weight.*
3. *Select any pair of subcubes* q_1 *of degree* d_1 *and* q_2 *of degree* $d_2 < d_1$ *if* $d_1 + d_2$; ***merge*** *them into a subcubes q of degree d if* $d_2 \leq n = deg$(Sparecube).
4. *Increment* d_1 *by 1. if* $d_1 \leq n$ *then go to step 2.*
5. *Execute the* ***Essential Tabular Process*** *(ETP) for all subcubes over all minterms.*

Modified QMA *for External Analysis*



Karnaugh Map
X: Don't Care

FCA	0	1	2	3	...
Imp1			V		V
Imp2	V			V	V
Imp3			V		V

Essential Table

Espresso

Example 1 of MQMA

Column Address

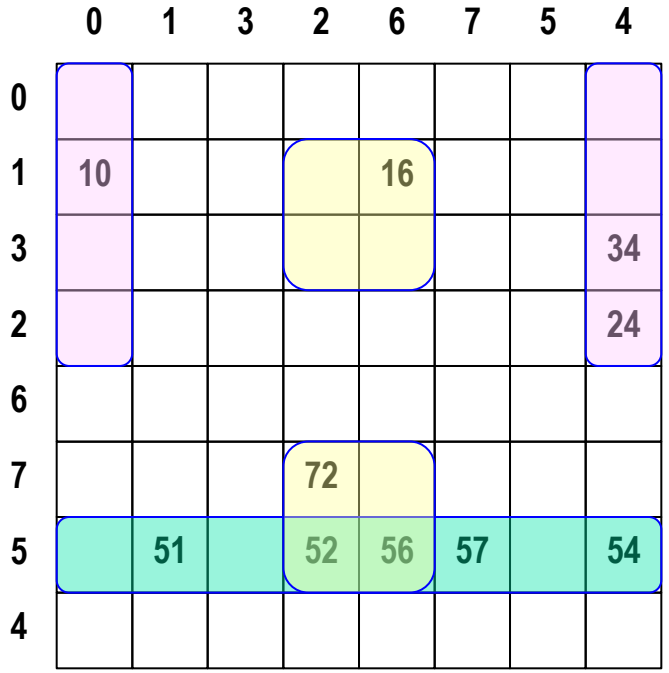
Row Address	0	1	2	3	4	5	6	7
0								
1	10						16	
2					24			
3					34			
4								
5		51	52		54		56	57
6								
7			72					

Ternary Sub-cube Address

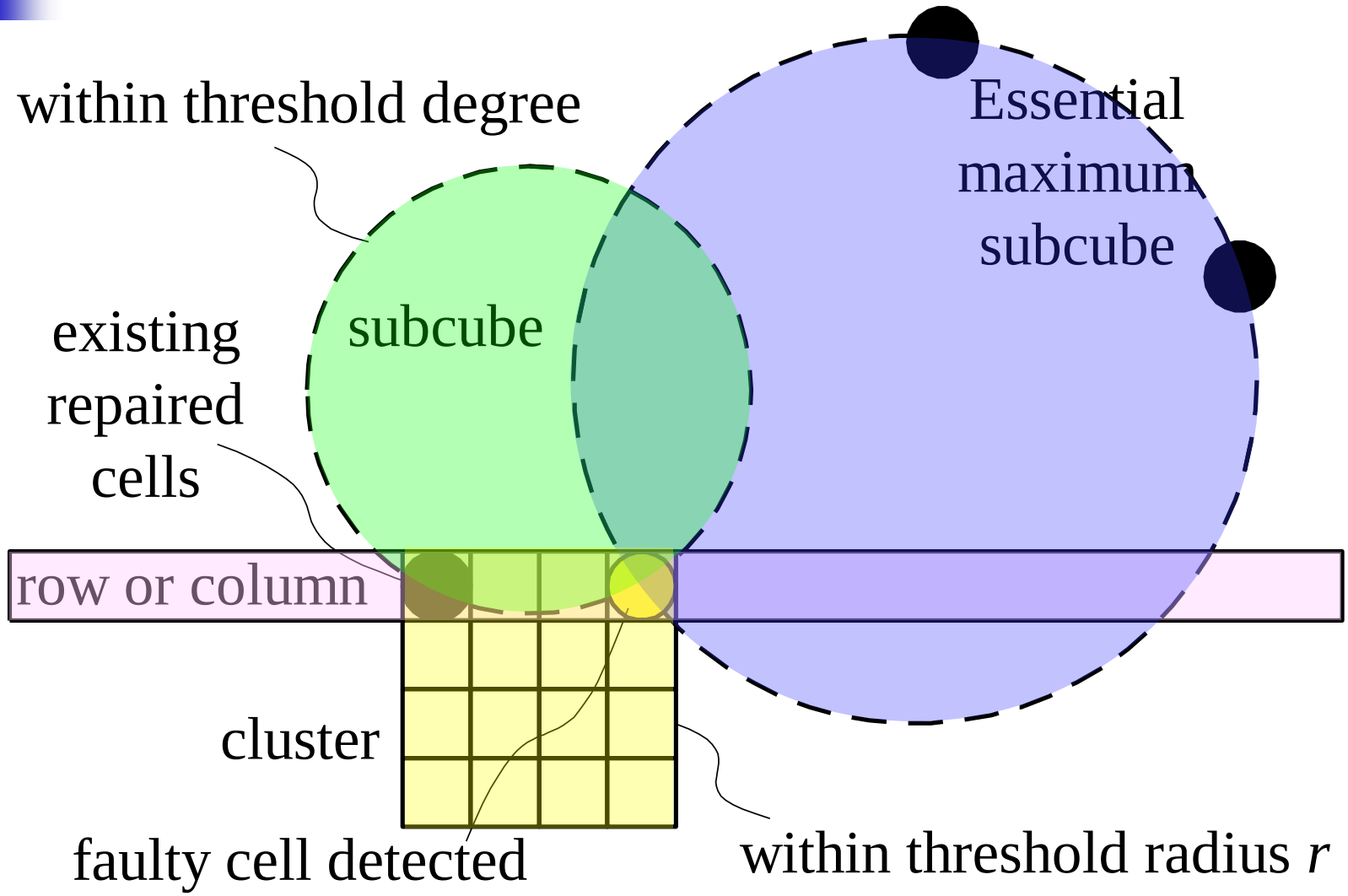
(Cell Address in Octal System)

	0	1	2	3	4	5	6	7	
0---00			10			24		34	S_0
101---		51	52		54		56	57	S_1
--1-10		16					72		S_2

- External Analysis
- Using an optimum algorithm – Modified Quine-McKluskey Algorithm



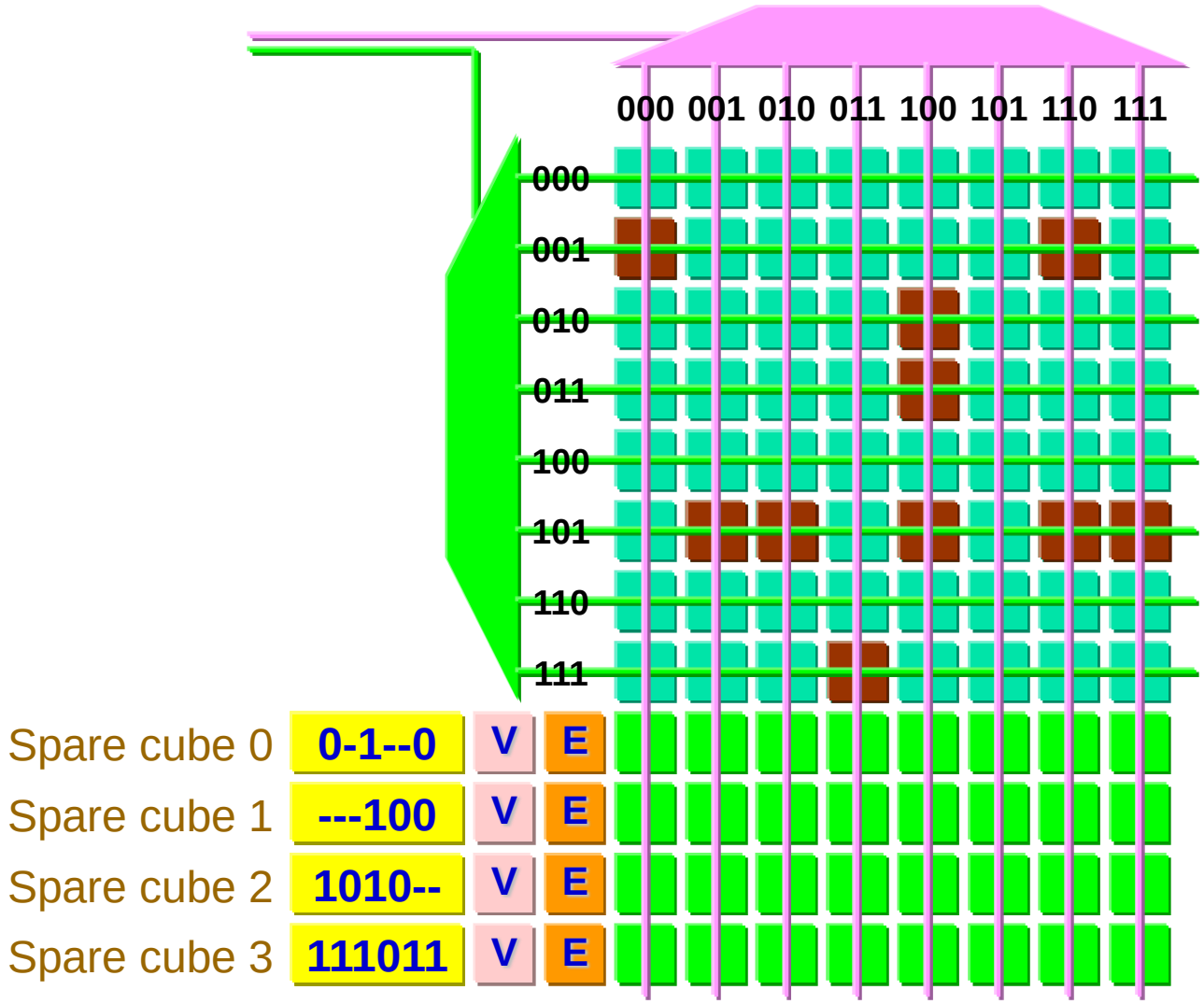
Heuristics of proposed ECPA



Proposed ECP Algorithm

```
 1  initialize;
 2  for each faulty cell address A{
 3      for each spare cube (C, V, E){
 4          if(V)
 5              if(E) repaired by merging A to C;
 6              else if A and C in a row/col/cluster(r) or d≤t<n
 7                      set Essential E and merge A to C;
 8          else set Valid V and store C = A;
 9          break;
10      }
11      if unrepaired for each non-essential cube C {
12          if(Max_dist(A, C)≤n) set Essential and merge A to C;}
13      if unrepaired, failed and exit;
14  }
15  expand non-essential cubes with degree n;
16  set all Essential;
17  success;
```

Example: Essential Cube Pivoting



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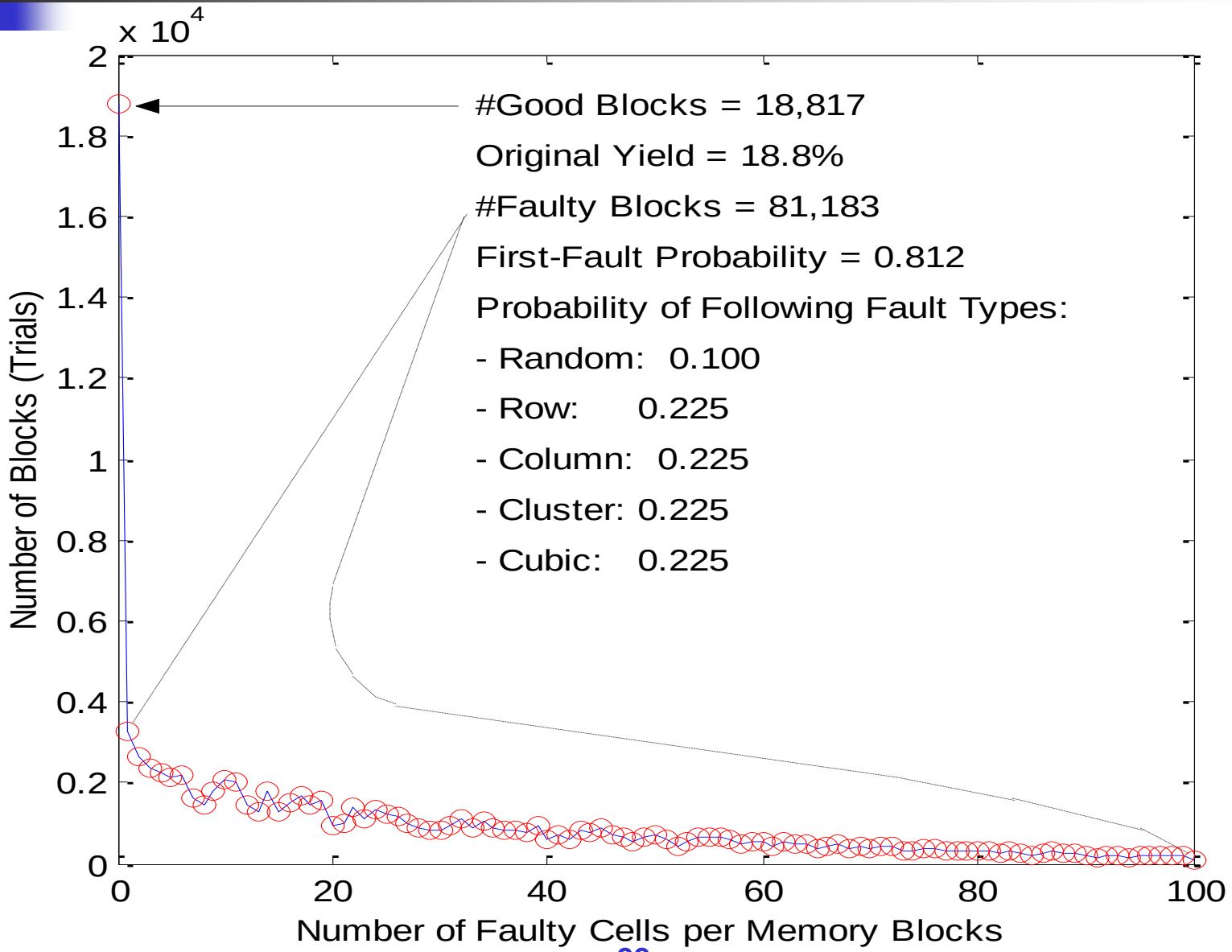
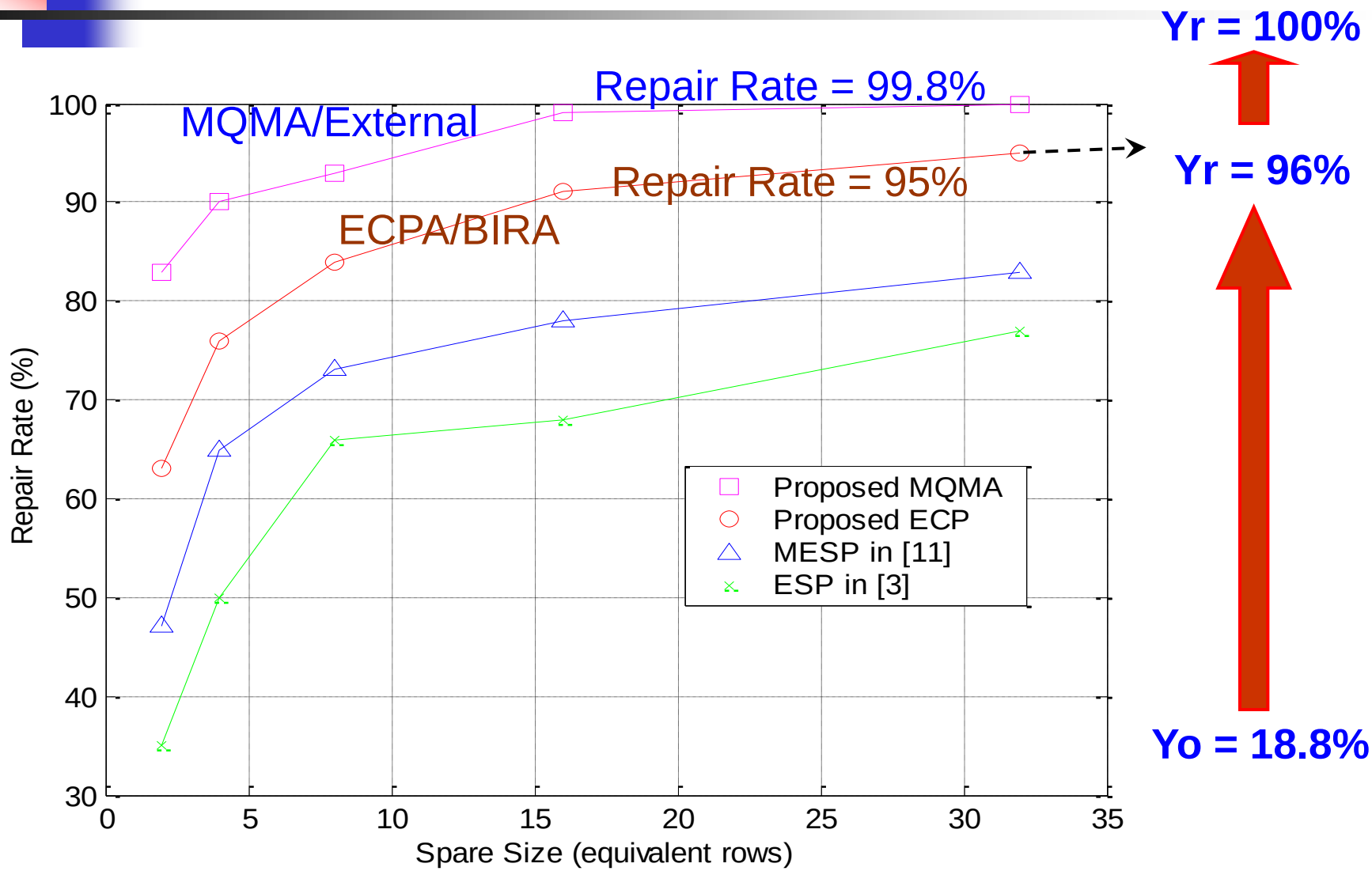
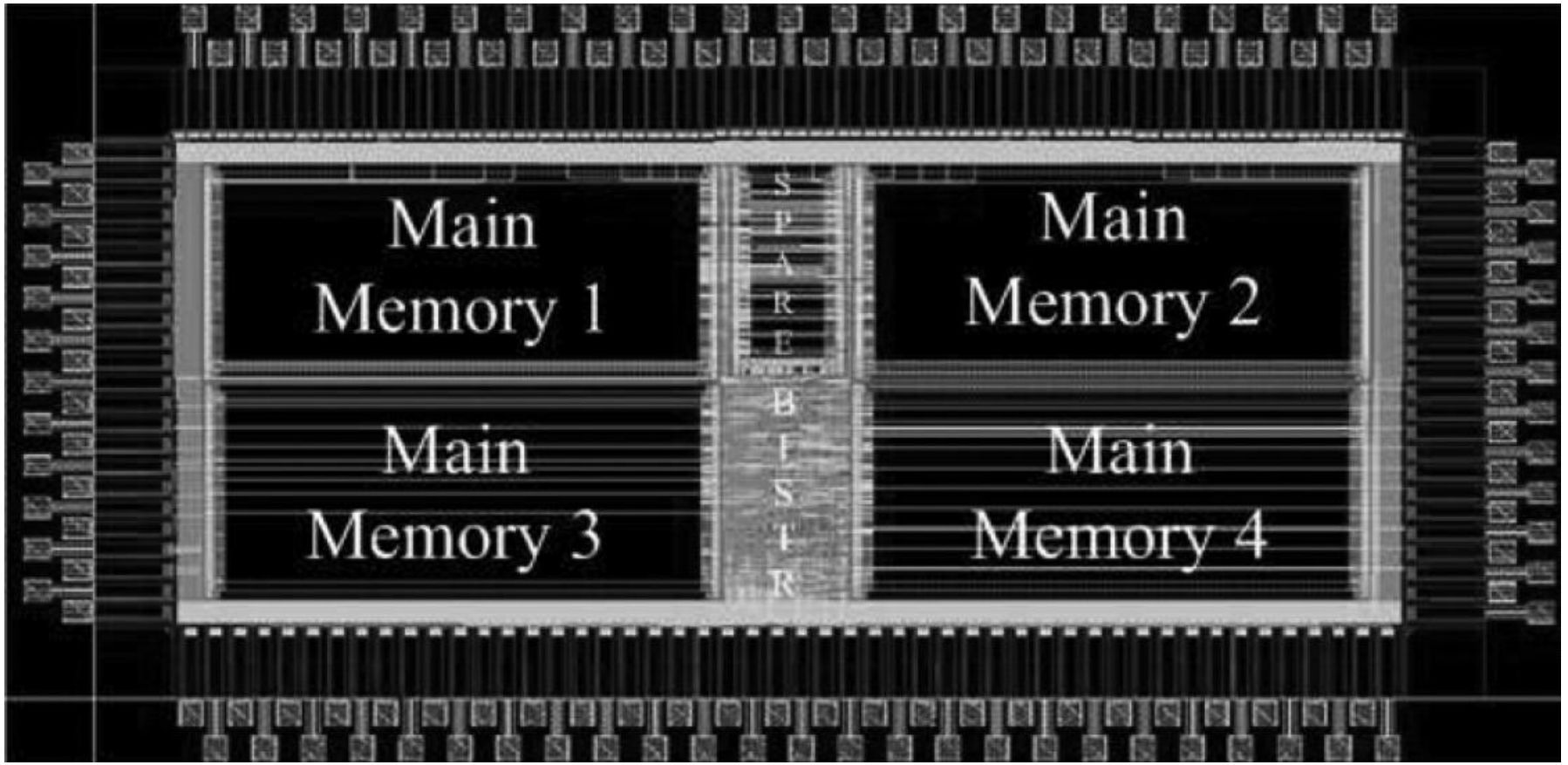
Case Study for Evaluation



Case Evaluation

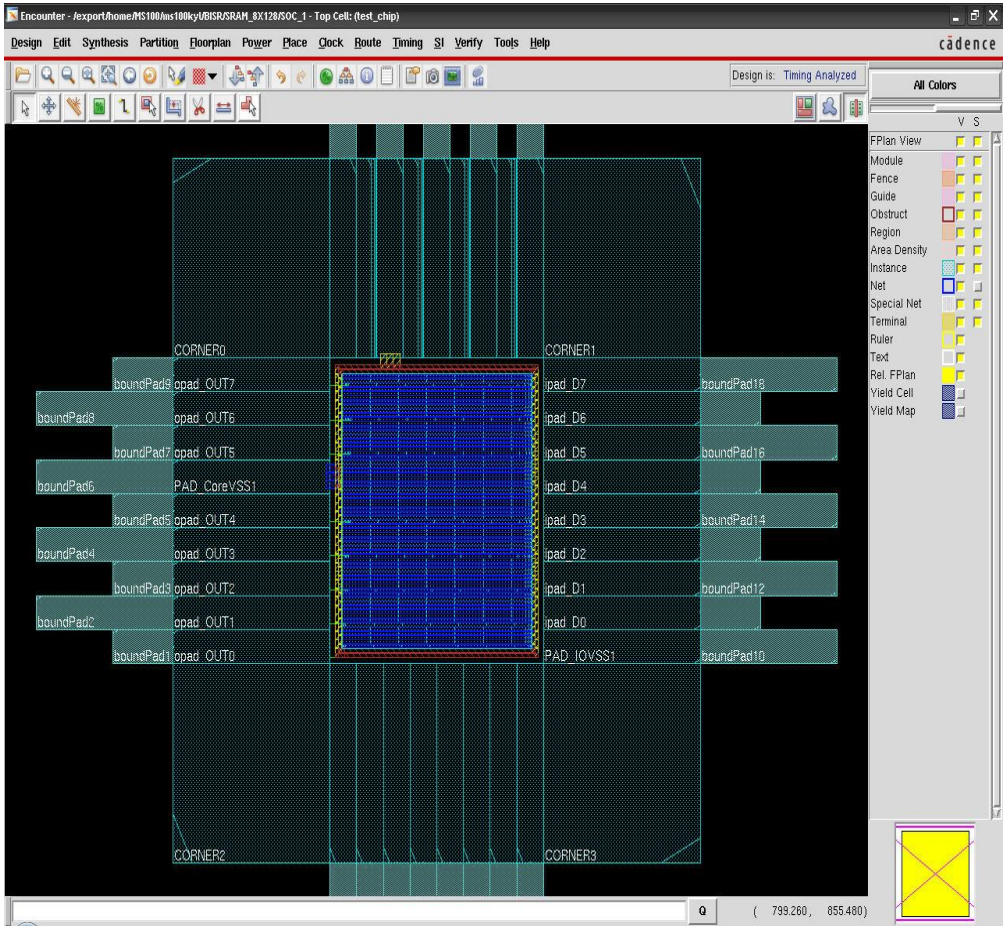


Layout (1/2) – A 16K-Word Case



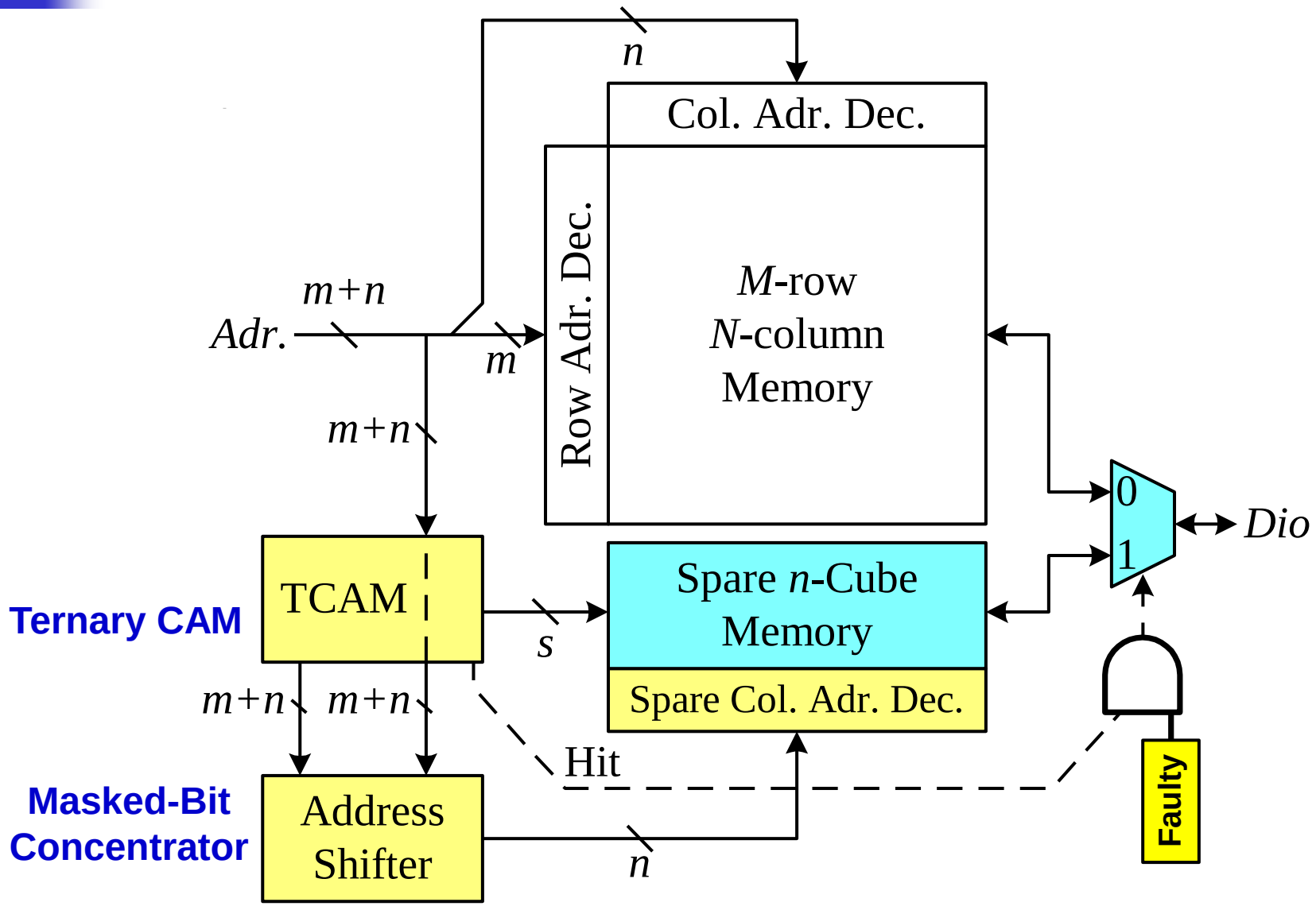
(TVLSI2010SKLu, followed-up)

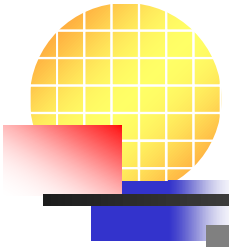
Layout (2/2)



- MBIST: HOY's BRAINS
- RF: Artisan's Compiler
- CBD: Synopsys's DC
- P&R: Synopsys's SE
- Editor: Virtuoso/Cadence
- Status:
  - ✓ Ready for small cases (128KB)
  - ✓ Tutorial available
  - ✓ Under verification
  - ✓ Tape-in on Aug.

Product Grading





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Conclusions

- A Hypercube-based Remapping Architecture and Efficient Algorithms are proposed.
- Repairing Rates can be highly improved up to almost 100%.
- Area overhead is small.
- Time penalty is still an issue.
- Effective yield can be still improved by sorting and disabling the access multiplexer for grade-A product.

Our “Sparrows”

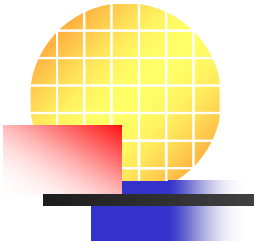
Small as the sparrow is, it possesses all its internal organs.

（麻雀雖小，五臟俱全）

-- *Chinese sayings*

References

1. A. Allan et. al. “Test and test equipment,” in 2009 technology roadmap for semiconductors, p.29, TST-6, 2009.
2. Y. Zorian and S. Shoukourian, “Embedded-Memory Test and Repair: Infrastructure IP for SoC Yield”, IEEE Design & Test of Computers, vol. 20, no. 3, May-June 2003, pp. 58-66.
3. C.-T. Huang, C.-F. Wu, J.-F. Li, and C.-W. Wu, “Built-In Redundancy Analysis for Memory Yield Improvement”, IEEE Trans. on Reliability, vol. 52, no. 4, Dec. 2003, pp. 386–399.
4. L.-T. Wang, C.-W. Wu and X. Wen. "VLSI Test Principles and Architectures." ISBN 10:0-12-370597-5, NY, Elsevier, 2006.
5. P. Mazumder and Y. S. Jih, “A new built-in self-repair approach to VLSI memory yield enhancement by using neural-type circuits,” IEEE Trans. CAD IC Circuits Syst., vol. 12, no. 1, pp. 24–36, Jan. 1993.
6. T. Kawagoe, J. Ohtani, M. Niiro, T. Ooishi, M. Hamada, and H. Hidaka, “A built-in self-repair analyzer (CRESTA) for embedded DRAMs,” in Proc. of IEEE International Test Conference, pp. 567-574, October 2000.
7. W. Jeong, T. Han and S. Kang. “An Advanced BIRA using parallel sub-analyzers for embedded memories.” In Proc. IEEE International SoC Design Conference, pp.249-252, 2009.
8. S. Hamdioui and A. J. van de Goor, “Efficient Tests for Realistic Faults in Dual-Port SRAMs”, IEEE Trans. on Computers, vol. 51, no. 5, May 2002, pp. 460-473.
9. Y. N. Shen, N. Park, and F. Lombardi, “Spare Cutting Approaches for Repairing Memories,” Proceedings of IEEE International Conference on Computer Design: VLSI in Computers and Processors, Austin, Texas, USA, pp.106-111, October 1996.
10. M. Lee and C.-W. Wu, “Method for Repairing Memory and System thereof.” ROC Patent No.200921690, disclosed on May 16, 2009.
11. S.-K. Lu, C.-L. Yang, Y.-C. Hsiao and C.-W. Wu. “Efficient BISR Techniques for Embedded Memories Considering Cluster Faults.” IEEE Trans. on VLSI, vol. 18, no.2, pp.184-193, 2010.
12. R. Nair, S.M. Thatte and J.A. Abraham , "Efficient Algorithms for Testing Semiconductor Random- Access Memories", IEEE Transactions on Computers, Vol. C-27, No. 6, June 1978, pp. 572-576.
13. P. Ohler, S. Hellebrand, and H.-J. Wunderlich, “An Integrated Built-In Test and Repair Approach for Memories with 2D Redundancy,” in Proc. of the 12th IEEE European Test Symposium, pp. 91-96, May 2007.
14. T.-C. Huang, “An Address Remapping Architecture and Memory Repairing Method thereof,” ROC Patent 99141225, Nov. 30, 2010.
15. M. Malek, A. Mourad and M. Pandya, “Topological Testing,” in Proc. International Test Conference, pp.103-110, 1989.
16. J. Bruck and C.-T. Ho, “Fault-Tolerant Cube Graphs and Coding Theory,” IEEE Trans. Information Theory, vol.42, no.6, pp.2217-2221, 1996.
17. K.E. Batcher, “Sorting networks and their applications,” in Proc. the AFIPS Spring Joint Computer Conference, vol.32, pp.307-314 , 1968.
18. M. S. Paterson, “Improved sorting networks with O(log N) depth,” Algorithmica vol.5, no. 1, pp. 75–92, 1990.
19. E. J. McCluskey, “Minimzatlon of Boolean functions,” J. Bell Syst. Tech., vol.35, no.5, pp.1417-1444, 1956.
20. L. Kraus and I. P. Batinic. “Built-in spare row and column replacement analysis system for embedded memories,” US Patent No. 6,304,989, Oct. 16, 2001.



Thank you for your attention!